Transport in fused InP nanowire device in dark and under illumination: Coulomb staircase scenario

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ABSTRACT

Electron transport is discussed for an ensemble of fused conical indium phosphide nanowires bridging two hydrogenated n^+-silicon electrodes. The current-voltage (I_d-V_d) characteristics exhibit a Coulomb staircase in dark with a period of ~ 1 V but it disappears under light illumination in some devices, while I_d-V_d is featureless smooth monotonic curve in other devices. It is shown that transport is dominated by a single NW pair in dark, while many NW pairs will contribute to transport under illumination.

Key words: InP, semiconducting nanowire, Coulomb staircase, illumination

1. INTRODUCTION – COULOMB STAIRCASE

Coulomb blockade devices have been an active research topic in the nanoscale device field [1-16]. When a device structure becomes small, a discrete nature of electrons plays an important role in transport, and a single electron moves from the source electrode, through a tiny "Coulomb lake", to the drain electrode. In the experimental efforts, the "Coulomb lake" has traditionally been created and controlled electronically, and Coulomb staircase devices so far have been all electronic. Here, we will present and report an *optically* controlled device for the fist time, to the best of authors' knowledge.

Defects/impurities are usually present in a crystal. When the device size is macroscopic, electrons will experience collisions, but eventually they can find an exit as schematically shown in Fig. 1(a). This is known as diffusive transport [17]. Collision to these obstacles causes friction to the electron motion, while the applied bias causes acceleration for the electrons. Because the friction is proportional to the velocity, the electron terminal velocity v is proportional to the acceleration, or it is proportional to the electric field E ($v = \mu E$, where μ is mobility). When the device geometry becomes much narrower vertically and shorter, a quasi-one-dimensional (1D) environment is realized and electrons must go through these obstacles. If there is only one obstacle which is too thick, no electrons can go through, and a tunneling (transmission) probability $|t|^2 = 0$. If it is thin, tunneling can occur with a finite $|t|^2$. If there are multiple obstacles, one may expect the entire tunneling probability is simply a product of each tunneling probability. This is generally true when the tunneling probability is high (tunneling resistance R_T << quantum resistance R_Q = 12.9 kΩ) or the charging energy of a "Coulomb lake" between two obstacles is low (a single electron charging energy $q^2/2C$ ~ thermal energy k_BT, where C is a lake capacitance). In these limits, the lake is not charged and the Coulomb repulsion effect is negligible as in Fig. 1(b).

In this article, we focus on the opposite limit, which is $R_T >> R_Q$ and $q^2/2C >> k_BT$ as in Fig. 1(c). Physically, this means that the lake can accommodate only an integer number of electrons because $R_T >> R_Q$ and an electron cannot coexist across the barriers. Adding an electron to the lake must be done against the Coulomb repulsion force in Fig. 1(d)

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because $q^2/2C >> k_BT$. This situation results in highly unusual (drain) current - (drain) voltage (I_d-V_d) characteristics – like a staircase as in Fig. 1(e). The voltage period of the staircase is related to the "Coulomb lake" capacitance.

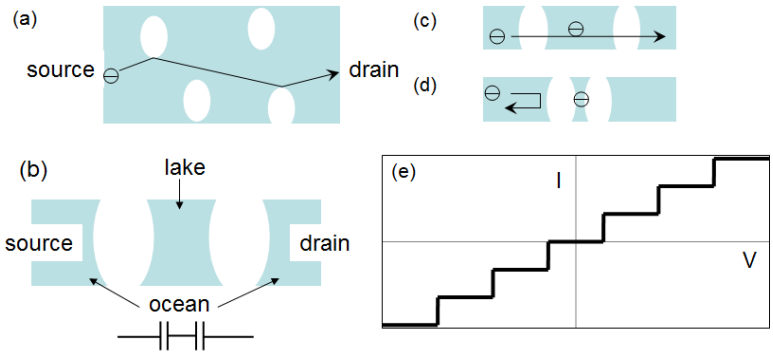

Figure 1. Transport of electrons (green) in defects/impurities (white ovals): (a) Macroscopic device with defects/impurities. (b) Definitions of conducting regions – source, lake, and drain. Source and drain are considered to be ocean with infinite number of electrons, but lake has a very small number of electrons. (c) Quasi-1D nanowire (NW) with two distant barriers, where the lake is large and an addition of another electron to the lake will not need large energy. Coulomb blockade is generally not relevant. An electron can go through without being influenced by a charge on the lake as indicated by an arrow. (d) Quasi-1D NW with two narrowly placed barriers. The Coulomb lake is so small that $q^2/2C >> k_BT$. Tunneling is quite rare so that $R_T >> R_Q$, resulting in an integer number of electrons on the "Coulomb lake." Under this situation, when another electron wants to tunnel in to the lake, it is associated with a hike in Coulomb repulsion potential. As a result, the second electron is pushed back by the first electron on the lake. This is Coulomb blockade. (e) Typical I_d-V_d characteristics of a Coulomb blockade device.

The unique shape of I_d-V_d itself is a scientific interest. Finding a relation between the observed voltage period in the staircase I_d-V_d and the "Coulomb lake" capacitance has been a core topic. Because of the highly nonlinear I_d-V_d characteristics, there are proposals to use it for electronic device applications. Nanoscale is significantly advantageous in fast operation with low power consumption, because charging up a device is achieved using *only a single electron*, which is the smallest possible charge amount the fundamental physics allows. Generally Coulomb blockade device structures are quasi-one dimensional (1D) and they provide simply a two-terminal device, where the staircase I_d-V_d cannot be controlled. Therefore, Tamura *et al.* considered placing a gate electrode to control the "Coulomb lake charge amount" [1]. By doing this, the device is now three-terminal and the staircase I-V can be controlled by gate bias.

In creation of devices, nanofabrication is absolutely necessary to control the tunneling barrier thickness and resultant magnitude of the tunneling resistance R_T of the system so that the condition, $R_T >> R_Q$ is achieved. The size of the "Coulomb lake" must also be precisely controlled through nanofabrication because the "Coulomb lake" capacitance must be small enough to guarantee $q^2/2C >> k_BT$. In many cases, achieving the second condition is not trivial, and thus, the device operation at low temperature down to the liquid helium temperature is mandatory. Placing a gate electrode to control the staircase I_d-V_d adds another step in nanofabrication, if people want to seek electrical methods to control the "Coulomb lake" charge.

Several devices exhibiting Coulomb staircase have been reported in the literature. Postma *et al.* used a carbon metallic carbon nanotube (CNT) with a pair of barriers created with atomic force microscope (AFM) [13]. The "Coulomb lake" was created between the barriers as in Fig. 2(a). The equivalent circuit was simply a pair of series connected capacitors. Hanna and Tinkham studied a system between the scanning tunneling microscope (STM) tip and metallic sample as in Fig. 2(b). The "Coulomb lake" was located between the STM tip and sample, and the equivalent circuit was again a pair of series connected capacitors. They proved it through their observation of I_d-V_d modulation when changing the STM-sample distance and resultant "Coulomb lake" capacitance [5]. Matsumoto *et al.* created a surrounding barrier and a resultant metallic "Coulomb lake" with pre-designed dimension by oxidizing a metallic layer with an STM tip as in Fig. 2(c). Because of the backgate structure, gate voltage was applied and it modulated the I_d-V_d characteristics. The equivalent circuit of a pair of series connected capacitors had a coupling capacitance to the "Coulomb lake." They confirmed that the staircase period was consistent with the "Coulomb lake" capacitance determined by the device geometry [9]. Thelander *et al.* created this gated quasi-1D InAs NW device in a backgate

structure and a pair of barriers were created with InP as in Fig. 2(d). The equivalent circuit was again a pair of capacitors and a gate capacitor linked to the "Coulomb lake." They showed the anticipated drain current behavior as a function of drain voltage and gate voltage [14]. In an extensive review by Kastner [6] and another by Likharev [11], many experimental efforts are also discussed. All of them require nanosculpture at least in one direction, if not two, to obtain quasi-1D structures, and the "Coulomb lake" and barriers are controlled with gate voltage. In this sense, the devices are all electronic.

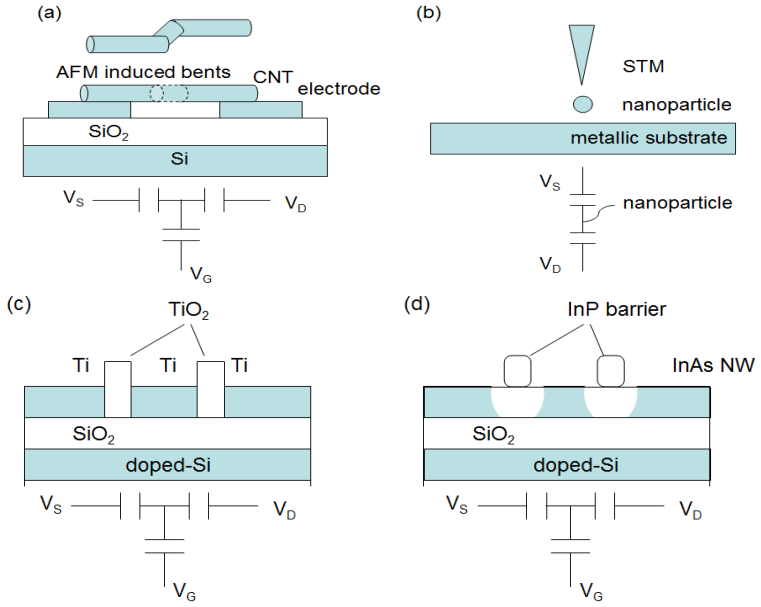

Figure 2. Experimental Coulomb staircase devices: (a) metallic CNT with a pair of AFM induced barriers placed on a pair of metallic electrodes in the backgate structure. (b) metallic nanoparticle placed on a metallic substrate measured with an STM tip. (c) TiO_2 surrounding barrier defining a Coulomb island on a Ti channel in the backgate structure. (d) InAs NW with a pair of barriers created with InP in the backgate structure.

2. CURRENT-VOLTAGE CHARACTERISTICS

Here, we consider a fused Indium phosphide (InP) nanowire (NW) device [18-21], where a small "Coulomb lake" and appropriate tunneling barriers are naturally created during the crystal growth process without specific nanofabrication process. Because of the extremely small "Coulomb lake," its relevant capacitance is so small that a room-temperature operation is possible. We will consider the control of the staircase via light illumination, so that we do not have to place another gate electrode to control the "Coulomb lake" charge. By carefully studying this system, we will obtain a material platform for Coulomb blockade device.

Kobayashi *et al.* reported InP nanowire synthesis and electrical transport measurements on a simple photoconductor under light illumination [18]. n^+ type hydrogenated silicon (n^+-Si:H) formed on a pair of metal electrodes separated with a gap served as templates for growing InP nanowires. InP nanowires were grown by low-pressure metal organic chemical vapor deposition with trimethylindium and phosphine used as precursors. The nanowires that nucleated randomly on the spatially-separated n^+-Si:H templates grew toward each other as shown in Figs. 2(a) and 2(b), as a result, some nanowires collided and fused together as shown in Fig. 2(c), establishing an electrical connection. Because of the n-type Si:H templates and the unintentionally doped InP nanowires that exhibited n-type conduction [19], electrons were the dominant carrier for electrical transport (We will discuss this in detail in the following sections). We performed detailed analysis of the DC electron transport characteristics of the InP nanowire photoconductors in darkness and under light illumination by laser light (633 nm, 1.95 eV) at various optical power levels up to 5 μW. The light energy is significantly greater than the InP direct bandgap E_g of 1.34 eV, thus appreciable electron-hole (e-h) pair generation was expected. One electrode was biased at V_d = -5 to 5 V while the other was grounded (thus designating them as the drain and the source, respectively), and the resulting I_d was measured. On an important note, the measurements were all taken at room temperature.

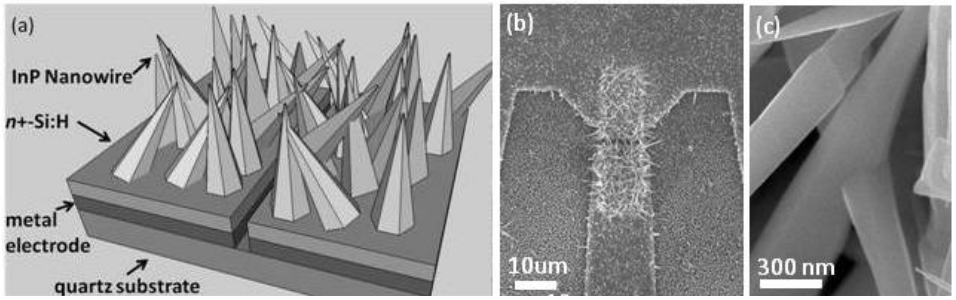

Figure 3. (a) Schematic of a fabricated InP nanowire (NW) photoconductor. (b) Scanning electron microscope (SEM) image (top view) of a representative InP NW photoconductor. InP NWs were selectively grown on the pair of n^+-doped Si:H electrodes. (c) SEM image of a point where two nanowires were fused.

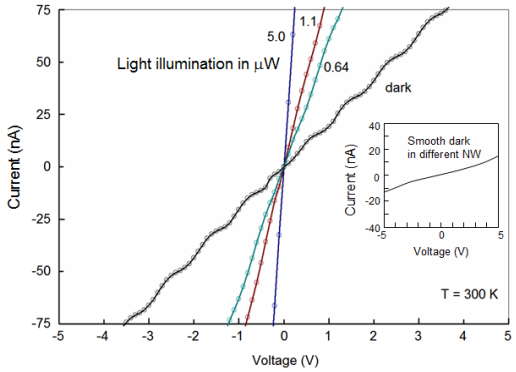

Figure 4. I_d as a function of V_d with light power as a parameter. The distinct staircase shape of the darkness curve is noticeable in contrast to the linearity of the illumination curves (with the possible exception of 0.64 μW). The staircase I_d-V_d characteristics are not always observed in all devices, and the inset shows such an example for a different device.

The resulting I_d-V_d plot is shown in Fig. 4 for various light illumination powers which are labeled in μW. Each μW increment increases the device conductance by 0.06 μS, and for 5 μW the conductance is increased by an order of magnitude. The functional forms, however, are significantly different when comparing the darkness I_d-V_d characteristics to any of the illuminated I_d-V_d characteristics. In the dark, I_d does not increase smoothly but rather has discrete jumps at regular intervals of V_d, giving the darkness I_d-V_d a distinct staircase shape. In order to extract the V_d period, we have subtracted the linear component of I_d and applied the Fourier transform to the result. The result has its peak at $\Delta V = 0.95$ V. Under light illumination at 0.64 μW, the staircase shape still exists but has become less prominent compared to the linear component, *i.e.* the V_d period has become shorter. Any further increase in illumination power erases the staircase and leaves the linear component, making the I_d-V_d characteristics Ohmic. In addition, the change is reversible: a device that has been illuminated will display, once returned to darkness, exactly the same staircase I_d-V_d as before.

We discuss the possible circuit equivalent circuit for the InP fused NW device. Multiple NW pairs bridge the electrodes. One pair is discussed first, whose structure is schematically shown in Fig. 5(a). The equivalent circuit is shown in Fig. 5(b). The fused NW circuit element is represented in rectangle and this will be discussed later. Usually finite resistance exists at each electrode contact and is represented by R_c. When two materials meet, there is a potential barrier at the contact, and electron transport is to go through that potential barrier. The potential barrier is effectively lowered by high doping. Depending on the nature of the barrier, transport can be simple diffusive [17], or tunneling [23], but in either case, current is a featureless simple monotonic function of voltage.

Although there is no discontinuity in the crystal orientation, there exist potential barriers as indicated in Fig. 5(c), and there is a "Coulomb lake." The mechanism for the existence of such potential barriers without any discontinuity in the crystalline structure can be understood using the electron wave transmission picture. When two wave guides meet as in Fig. 5(c), there is always a finite reflection of the wave since the wave a sees different environment at the fused portion. The existence of the reflected wave can be translated to an existence of the potential barrier at the fused portion. It is possible to evaluate the change in the Fermi level in dark and under light illumination. Accordingly, the barrier

height is estimated to be 25-85 meV [21, 22]. Electrons will tunnel through barriers and move from one NW to the other. The size of the "Coulomb lake" is about ~10 nm^2 × 0.5 nm, corresponding to ~0.1 aF of capacitance [21, 22]. The active regions with mobile electrons present are depicted with blue. In dark, the electron Fermi level is low, and the "Coulomb lake" is well isolated from the electron oceans as in Fig. 5(d). The equivalent circuit is a pair of capacitances connected in series, and this can generate Coulomb staircase characteristics. However, when the light is illuminated, the Fermi level is raised due to e-h creation, and the potential barriers are buried. Depending on the device, the potential barriers may not be appropriately formed and the "Coulomb lake" may not be isolated well. In this case, the equivalent circuit is a resistor even in dark, and the staircase I_d-V_d characteristics are not observed. The fused portion behaves as a simple resistor as in the figure. In our InP NW devices, this Fermi level modulation is done optically, *i.e.,* with light illumination. In previous devices, this is done using the gate electronically, through the gate modulation effect by applying gate voltage.

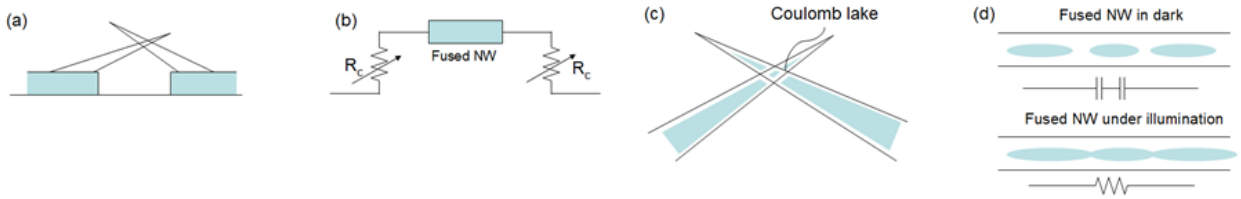

Figure 5. Schematic diagrams of the pair of tunneling barriers responsible for the experimental I_d-V_d characteristics for (a) darkness, (b) light illumination power small enough to still produce a staircase, and (c) power large enough to make the staircase disappear. The height of the barriers should be higher than 26 meV so that the system is not overridden with thermal noise. In order to ensure a staircase, the barriers must provide tunneling resistance greater than 12.9 kΩ so that an electron cannot coexist in the island (middle) and in the source or drain (outside the barriers).

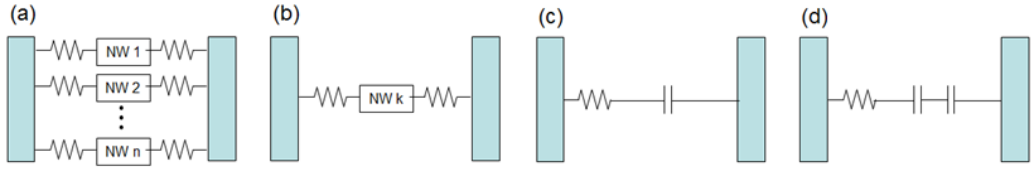

Figure 6. Equivalent circuits for InP fused NW device. (a) Equivalent circuit with multiple InP NW pairs bridging the electrodes. (b) Equivalent circuit with a dominant (most conductive) InP fused NW. (c) Equivalent circuit with s single tunneling barrier at the fused portion, resulting in smooth I_d-V_d characteristics. (d) Equivalent circuit with a pair of tunneling barriers at the fused portion, resulting in staircase I_d-V_d characteristics.

In our InP NW device, there are multiple fused NW pair bridges as in Fig. 6(a). Since there are tunneling barriers at the fused portion and tunneling barriers are different from one NW pair to another, there is a significant conductance variation. Eventually only one NW pair (k) is dominant as in Fig. 6(b). In fact, the conductance G_i of NW pair is related to the barrier thickness w_i by

$$G_i = G_0 \exp(-2\kappa w_i) \ , \tag{1}$$

where G_0 is a conductance in the absence of the tunneling barrier and κ is the imaginary wavelength in the tunneling barrier region. Let the probability function of w be $P_w(w)$. Then the probability function $P_G(G)$ for conductance G if we know the tunneling barrier probability function $P_w(w)$ is given by

$$P_G(G) = P_w(w) \left| \frac{dw}{dG} \right| = \frac{P_w(w)}{2\kappa G_0 \exp(-2\kappa w)} = \frac{P_w(w)}{2\kappa G} \ . \tag{2}$$

There are no experimental data available for $P_w(w)$. If w appears with a similar probability between w_{min} and w_{max}, then $P_w(w)$ is a box-car function. This quasi-uniform probability distribution is often used in the analysis of fabrication processes, when the Gauss distribution is inappropriate. In fact, the Gauss distribution does not exclude unsuitably small or large w values and is not appropriate in many cases, including our case. Then, P_G essentially behaves as $1/G$. This means that many NW pairs with small G values appear in group. However, a high G value pair appears in an isolated

manner. Although there are multiple NW pairs, highly likely, only one NW pair will be responsible for transport. It has to be emphasized this conclusion is true *only in dark*. Under light illumination, the Fermi level is raised and tunneling barriers are buried. Then, tunneling transport is no longer important and there is no single NW pair dominance.

We combine two contact contributions. Depending on whether the "Coulomb lake" is well defined or not, there are two possible cases. If the "Coulomb lake" is not well defined, there is a single tunneling barrier and the equivalent circuit is as shown in Fig. 6(c). The device will show a smooth I_d-V_d curve even in dark. However, if the "Coulomb lake" is well defined, there are a pair of tunneling barriers and the equivalent circuit is as shown in Fig. 6(d). The device will show a Coulomb staircase in dark.

3. CONCLUSION

We have analyzed DC I_d-V_d measurements of a device with multiple fused InP NWs bridging the gap between two n^+-Si:H electrodes in darkness and under various powers of light illumination. The darkness curve exhibits a distinct staircase shape and it is explained by the Coulomb staircase mechanism. Multiple NW pairs bridge the electrodes, but because of the tunneling transport in each NW pair, only one NW pair will have a dominant conductance and the device characteristics in dark is eventually determined by that NW pair. Under the light illumination, the Fermi level is raised and tunneling barriers are buried. Thus, multiple NW pairs equally contribute to transport.

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