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Single Crystal Nanowire Vertical Surround-Gate Field-Effect Transistor

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ABSTRACT

Harnessing the potential of single crystal inorganic nanowires for practical advanced nanoscale applications requires not only reproducible synthesis of highly regular one-dimensional (1D) nanowire arrays directly on device platforms but also elegant device integration which retains structural integrity of the nanowires while significantly reducing or eliminating complex critical processing steps. Here we demonstrate a unique, direct, and bottom-up integration of a semiconductor 1D nanowire, using zinc oxide (ZnO) as an example, to obtain a vertical surround-gate field-effect transistor (VSG-FET). The vertical device structure and bottom-up integration reduce process complexity, compared to conventional top-down approaches. More significantly, scaling of the vertical channel length is lithographically independent and decoupled from the device packing density. A bottom electrical contact to the nanowire is uniquely provided by a heavily doped underlying lattice-match substrate. Based on the nanowire-integrated platform, both n- and p-channel VSG-FETs are fabricated. The vertical device architecture has the potential for use in tera-level ultrahigh-density nanoscale memory and logic devices.

As device dimensions continue to shrink into the nanometer length scale regime, fundamental physical limits and economics are likely to hinder further scaling according to Moore's law.[1] New strategies including usage of new materials, innovative device architectures, and smart integration schemes are needed to extend the current capabilities beyond the end of the technology roadmap time frame.[2] "Bottom-up" approaches to nanoelectronics that utilize functional electronic nanostructures,[3−5] in particular 1D semiconductor nanowires, have the potential to stretch beyond the limits of traditional top-down manufacturing. However, the usual pick-and-place approaches of manipulating and aligning horizontally lying nanowires to fabricate prototype devices and the stringent lithography requirements have to be overcome before practical realization of integrated nanosystems. Furthermore, lithographic issues become paramount in further scaling of these nanowire-based planar devices, especially in defining ultra-small channel length in field-effect transistors (FETs).

A proposed solution to these problems is to grow single crystal 1D nanowires directly on a device substrate with the major nanowire growth axis orthogonal to the substrate plane and to use this nanowire-integrated platform for direct device fabrication. Based upon this vertical generic configuration, an ensemble of nanoscale devices can be realized[6,7] (Figure S1, Supporting Information). In the present work, we demonstrate the potential of this approach through the realization of a vertical surround-gate field-effect transistor (VSG-FET), which takes advantage of the vertical dimension unlike planar nanowire-based FETs and traditional metal-oxide-semiconductor (MOS) FETs. The advantages of this vertical device configuration and enhanced device performance have been addressed recently.[8,9] In addition, 1D nanowires obtained using the bottom-up approach completely eliminate the demanding lithography and etching processes typically employed in the top-down approach to obtain nanopillars.[10,11]

To obtain vertically aligned 1D ZnO nanowire arrays directly on substrates, we used a well-established method involving a combination of carbothermal reduction and gold (Au) catalyst-mediated heteroepitaxial growth approach.[12] Briefly, the feedstock source consists of a mixture (1:1 by weight) of zinc oxide (purity 99.99%) and graphite powder (purity 99.99%). The substrate was placed downstream (∼1−3 cm) from the feedstock source in a quartz boat, which was placed in a horizontal tube furnace while a constant flow of argon gas (30 sccm, purity 99.999%) was maintained. After 15 min of equilibration, the temperature was ramped at a rate of 1 °C/s to a preset incubation temperature of 925 °C. The entire setup was cooled to room temperature before retrieving the samples for structural characterization and device processing. Similar techniques have been used to obtain a variety of other directional nanowires with different chemical compositions[6,13] on various substrates. Micro- and nanocontact soft lithography[14] were employed to pattern the

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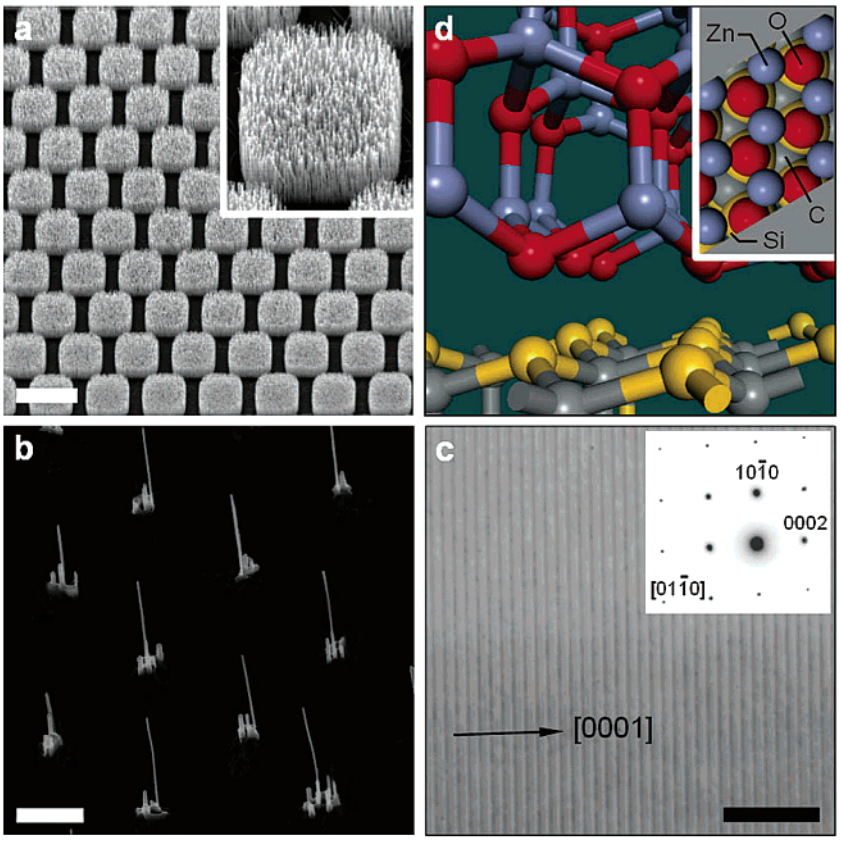

Figure 1. Vertical ZnO nanowire arrays on SiC epilayered substrates. (a) A 45° perspective FE-SEM image of an array of nanowires on SiC substrate. The inset shows a zoom-in FE-SEM image, revealing high density of nanowires within each catalyst pad. (b) A 45° perspective FE-SEM view of an array of individual ZnO nanowires sprouting from each catalyst spot. (c) An HRTEM image showing sharp lattice fringes with an interplanar spacing of ~5.45 Å, corresponding to the {0001} plane of ZnO. The inset shows an SAED pattern taken perpendicular to the stem of the nanowire, indicating (by the arrow) [0001] as the nanowire growth direction. (d) Schematic view of optimized interfacial molecular geometry between the ZnO(0001)−SiC(0001) interface. The inset shows preferential epitaxial stacking of oxygen atoms of ZnO on the topmost silicon layer of SiC. Scale bars: 10 μm, 1 μm, and 5 nm for a, b, and c, respectively.

Au catalyst arrays in strategic locations on a heavily doped ($>10^{18}$ cm^{-3}) silicon-terminated silicon carbide (SiC) epilayer on either 4H− or 6H−SiC substrates. Other techniques such as e-beam lithography and UV lithography have also been used with success.

Figure 1a shows a field-emission scanning electron microscopy (SEM) image of highly regular arrays of vertically aligned ZnO nanowires from micro-patterned Au pads. Uniform coverage of the nanowires is typically observed on the entire substrate where the Au catalysts are. A zoom-in perspective SEM image (inset of Figure 1a) reveals high density (~100/μm^2) of ZnO nanowires within each catalyst pad (7 μm × 7 μm). However, for most applications in nanoelectronics and optoelectronics, controlling the number density of the nanowires is important. This can be achieved by controlling the diameter and thickness of the catalyst pad. From repeated experiments with different diameters and thicknesses of the Au catalyst pads, we found a threshold diameter (d_{th}) of ~200 nm and thickness (t_{th}) of ~15−20 Å that facilitate a single ZnO nanowire growth at each catalyst spot. Figure 1b shows a regular array consisting of an individual nanowire at each catalyst spot with $d \sim 200$ nm and $t \sim 20$ Å. The typical average diameter of the nanowires is 40 ± 5 nm and the average vertical growth rate is ~1 μm/hr. A high-resolution transmission electron microscopy (HRTEM) image, as shown in Figure 1c, further reveals sharp lattice fringes with an interplanar spacing of ~5.45 Å, corresponding to the {0001} plane of ZnO. A highly ordered selected-area electron diffraction (SAED) pattern (inset of Figure 1c), taken perpendicular to the longitudinal growth axis of the nanowire, reveals its high single crystallinity. The regular diffraction spots could be indexed to the $[01\bar{1}0]$ zone axis of hexagonal ZnO and the growth direction is determined to be [0001], parallel to its *c*-axis.

The motivations for using SiC as the device substrate for the ZnO nanowires are as follows. First, a good interfacial lattice match between the major epitaxial crystal plane of the nanowires and the substrate is crucial in facilitating the growth of vertically oriented single-crystal nanowires based on the vapor−liquid−solid mechanism.[15] In the present case, the minimum lattice mismatch (~5.5%) between ZnO (0001) and hexagonal SiC (0001) is predicted to promote vertically aligned growth of ZnO nanowires as confirmed in Figures 1a and b. A schematic view of the optimized interfacial molecular geometry between ZnO (0001) on Si-terminated SiC (0001) with an interfacial interaction energy of approximately −3631.30 kJ/mol is shown in Figure 1d. The inset further reveals preferential stacking of oxygen atoms of ZnO (0001) on the topmost silicon layer of SiC (0001).[16] Second, for device architectures that require bottom electrical

contacts to the nanowires, a conductive substrate is highly desirable. SiC substrates can be heavily doped to become highly p- or n- type. Although it has been shown that *a*-sapphire[17] and highly oriented pyrolytic graphite[12] provide excellent lattice match with *c*-plane of ZnO and that vertical nanowires can be achieved, they suffer from the fact that they are either nonconductive or are incompatible with existing device processing. Third, SiC has a very high thermal conductivity (~4.9 W cm^{-1} K^{-1}), high saturated electron drift velocity (~2.7 × 10^7 cms^{-1}), and high breakdown electric field strength (~3 MV^{-1}). It is also a material of choice for high temperature, high voltage, high frequency, and high power applications.[18] With ZnO as a radiation-hard and optoelectronic material, the combination of both could potentially be used for a wide range of commercial and space applications ranging from nanoelectronics to optoelectronics.

The bottom-up nanowire-integrated substrate can potentially provide a versatile generic platform for direct integration to obtain functional nanodevices (Figure S1). Next, we demonstrate the fabrication of a ZnO-based VSG-FET. For practical applications, addressable patterned underlying electrical contacts may be used. However, for single device demonstration, a SiC substrate (5 × 5 mm) with a Au catalyst spot (~180 nm in diameter, 15 Å in thickness) patterned by e-beam lithography was employed prior to nanowire growth. Figures 2a−f show schematically a generic process flow outlining the major steps leading to a functional *p*-VSG-FET. In principle, similar fabrication schemes can be used with other nanowire/substrate combinations. We began with a nanowire-integrated substrate as shown in Figure 2a. The ZnO nanowire functions as the active channel while the underlying p^+-SiC (> 10^{18} cm^{-3}) epilayer serves as the source electrode of the *p*-VSG-FET. The typical diameter and height of the nanowire were respectively ~40 and ~1000 nm. Note the terminating Au catalyst head which was brought along with the nanowire growth. Unlike the traditional top-down approach relying on reactive-ion etching, the favorable straight sidewall profile of the nanowire is well-maintained. Figure 3a shows an SEM image of a ZnO nanowire on a p^+-SiC/4H−SiC substrate. Interestingly, the nanowire grew vertically from a "dome"-like hexagonal base, as can be seen from the top view SEM image (inset of Figure 3a). Similar results have been observed on the n^+-SiC epilayer, which is used in fabrication of *n*-VSG-FET. We attribute this to the formation of a buffer layer which relaxes the lattice mismatch between ZnO (0001) and SiC (0001) prior to 1D nanowire growth.

Next, we subjected the platform to a silicon dioxide (SiO_2) chemical vapor deposition process (CVD)[19] (Figure 2b) using tetraethylorthosilicate as the precursor at an elevated temperature of 700 °C whereby ZnO nanowire was conformally surrounded and encapsulated with a thin layer of SiO_2 (~20 nm), which serves as the gate oxide of the *p*-VSG-FET. This is a critical step since nonconformal coverage of the ZnO nanowire can lead to subsequent large gate leakage current and eventual device failure. This was then followed by a conformal ion-beam deposition of Cr metal (~40 nm)

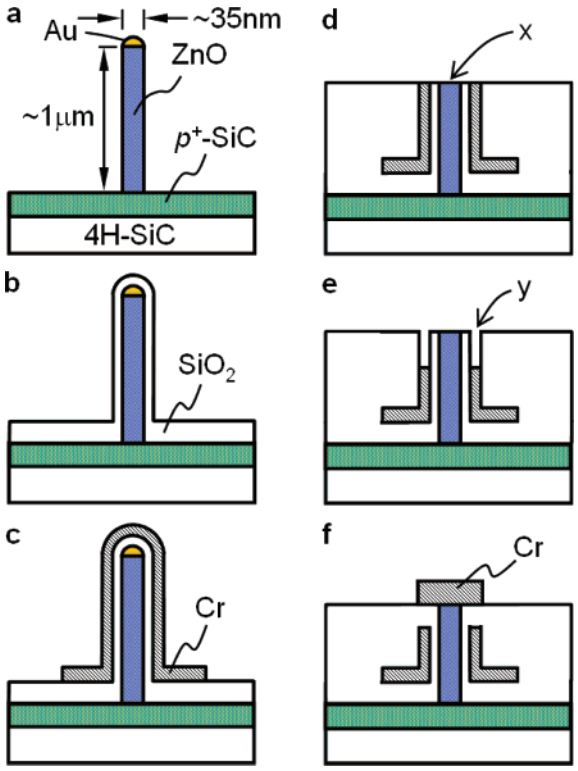

Figure 2. Vertical surround-gate field-effect transistor (VSG-FET) process flow. (a−f) Schematic of a process flow showing the major steps taken to fabricate a ZnO nanowire-integrated *p*-VSG-FET. Cross-sectional views are shown for the various critical fabrication stages. (a) A vertical ZnO nanowire-integrated p^+-SiC/4H−SiC substrate. The underlying p^+-SiC epilayer serves as the bottom source while the vertical ZnO nanowire acts as the active hole channel. (b) Surround-gate oxide formation. Conformal chemical vapor deposition (CVD) of thin film of silicon dioxide (SiO_2) ~ 20 nm was performed to clad the nanowire. (c) Surround-gate electrode formation. Conformal ion-beam deposition of chromium (Cr) metal (~40 nm) surrounding the gate oxide. (d) Active channel length formation. SiO_2 CVD was used to completely encapsulate the nanowire and was followed by chemical mechanical polishing (CMP) to remove the excess SiO_2, thus exposing the tip of the nanowire (denoted by x) and the Cr surround-gate electrode. Note that the Au alloyed head was also removed during the CMP process. (e) Recess formation. A recess ~30 nm was introduced by selective Cr wet etching (denoted by y). (f) Formation of top Cr gate electrode (~100 nm thickness). The recess was filled by SiO_2 CVD, followed by CMP to expose only the tip of ZnO nanowire and top Cr drain electrode formation.

surrounding the SiO_2-encapsulated ZnO nanowire as shown in Figure 2c. Figure 3b shows an SEM image of a Cr(10 nm)/SiO_2(20 nm)/ZnO nanostructure. We have observed that vertical directionality of the nanostructures is typically retained for nanowires with aspect ratio ~20, beyond which the cladded nanostructures bend away from the substrate normal. A further SiO_2 CVD step followed by a chemical mechanical polishing (CMP) step were performed to planarize and fully expose the top of the nanowire (denoted x) and the Cr surround-gate electrode as shown in Figure 2d and Figure 3c. The latter shows the highly conformal cladding of the SiO_2 gate oxide and the Cr electrode surrounding the ZnO nanowire. This planarization step served both to remove the Au alloyed head and define the vertical channel length of the *p*-VSG-FET. Demanding lithography

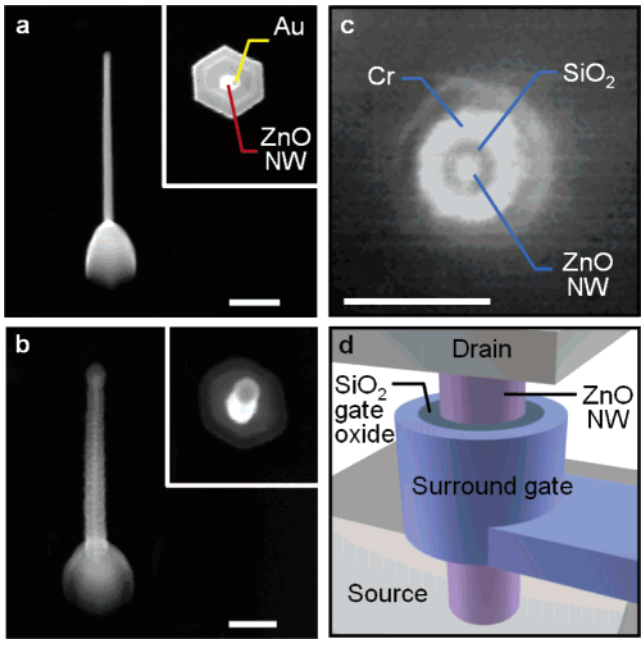

Figure 3. FE-SEM micrographs of cladded ZnO nanowires. (a) A vertically aligned ZnO nanowire projecting from a "dome"-like ZnO buffer layer. The inset shows its top-view FE-SEM image, revealing the hexagonal geometry of the buffer layer. (b) The same nanowire cladded with Cr(10 nm)/SiO_2(20 nm) layers. Corresponding top-view FE-SEM image shows broadening of the diameter of the cladded ZnO nanostructure. The hexagonal base can still be clearly seen. (c) Top view FE-SEM image of the cladded ZnO nanostructure prior to recess formation and deposition of the top Cr drain electrode. The surround-gate oxide and Cr gate electrode can be clearly observed, showing the highly conformal CVD and ion-beam deposition processes. (d) A 3D schematic illustrating the critical components of VSG-FET. Scale bar: 200 nm for a, b, and c.

and complex active channel processing schemes are hence completely eliminated.

As shown in Figure 2e, a recess (denoted y) ~30 nm was introduced in the Cr surround-gate by selective wet chemical etching of Cr.[20] This was followed by SiO_2 CVD to fill in the recess and a CMP step to expose only the tip of ZnO nanowire prior to laying down a top Cr electrode (100 nm thickness), which constitutes the drain electrode of the *p*-VSG-FET (Figure 2f). These particular steps avoid direct electrical contact between the Cr gate and top drain electrodes. Sufficient recess was performed to minimize large overlap capacitance between the gate and drain electrodes, which can be crucial in high-frequency applications. Figure 3d shows a 3D schematic illustrating the various critical components of a completed VSG-FET. A cross-sectional SEM image of the VSG-FET illustrating a side view of the as-fabricated nanotransistor is shown in the inset of Figure 4c, which reveals an active channel length ~200 nm. The channel length can be adjusted by varying the CMP processing durations and conditions without the help of lithography, in addition to controlling the height of the nanowire by the growth time (and hence the device channel length).

The device characteristics of a *n*-VSG-FET and a *p*-VSG-FET are shown in Figure 4. Figures 4a and b show the drain current I_{ds} vs drain voltage V_{ds} profiles obtained with the *n*- and *p*-VSG-FETs, respectively, for different gate bias V_{gs}. In the *n*-VSG-FET, I_{ds} increases with increasing positive V_{gs}, and this is characteristic of electron transport. The *n*-VSG-FET is normally on and turns off at $V_{gs} = -3.5$ V, which is the threshold voltage (V_{th}). This is attributed to the ZnO channel, which is unintentionally doped to be *n*-type in air, possibly due to oxygen deficiency and/or interstitial Zn.[21] In the *p*-VSG-FET, I_{ds} increases with increasing negative V_{gs}, and this is characteristic of hole transport. The *p*-VSG-FET has a V_{th} very close to zero, 0.25 V, in contrast to the normally on *n*-VSG-FET.[22] Nevertheless, in both cases, I_{ds} vs V_{ds} profiles reveal a rapid increase of $|I_{ds}|$ with $|V_{ds}|$, i.e., the absence of I_{ds} saturation. This literally indicates that neither the traditional channel pinch-off nor the carrier velocity saturation[23,24] is relevant in the VSG-FET operation. The absence of I_{ds} saturation can be related to the electrode contact effects, which will be reported later. The transconductance per nanowire is 50 nS and 35 nS at $|V_{ds}| = 1$ V for the *n*- and *p*-channels, respectively. A high on-to-off current ratio of $I_{ON}/I_{OFF} > 10^4$ is observed for the *n*-VSG-FET, while a respectable $I_{ON}/I_{OFF} > 10^3$ is observed for the *p*-VSG-FET.

Figure 4c shows I_{ds} vs $|V_{gs} - V_{th}|$ characteristics of $V_{ds} = 1.0$ V for the *n*-channel, and $V_{ds} = -1.0$ V for the *p*-channel VSG-FETs. The former shows a linear dependency, while the latter shows a strong nonlinearity, where I_{ds} increases more rapidly with increasing $|V_{gs} - V_{th}|$. This can be understood by noting that not all charges induced by V_{gs} can contribute to charge transport. The surround cylindrical gate capacitance C_g is estimated by $C_g = 2\pi\epsilon_{ox}\epsilon_0 l/\ln(b/a)$, where l is the nanowire length, a is the nanowire diameter, and b is the coaxial diameter of the SiO_2 with dielectric constant ϵ_{ox}.[25] Figure 4d is a schematic cross-section of the *n*-channel (left) and *p*-channel (right) of the VSG-FETs where the top drain and bottom source electrodes are not shown. In the *n*-channel, the variation of gate-induced charge dQ due to dV_{gs} involves essentially electrons that are mobile in the channel. I_{ds} is simply proportional to the electron density, and this explains the observed linearity in the I_{ds} vs $|V_{gs} - V_{th}|$ profile. However, in the *p*-channel, dQ involves both holes and ionized impurities in the depletion region.[26] Only holes can contribute to charge transport and the ratio of holes (to ionized impurities) in the channel becomes higher as V_{gs} becomes negatively larger. This could constitute the mechanism for the observed *p*-channel nonlinearity.[27]

Using $|Q| = C_g|V_{gs} - V_{th}|/l$ with $a = 16$ nm, $b = 40$ nm, and $l = 200$ nm, we obtain $|Q|/e = 1.9 \times 10^7$ cm^{-1} at $|V_{gs} - V_{th}| = 2$ V. Thus, the effective electron and hole mobility is estimated as $\mu_e = 0.53$ cm^2/Vs and $\mu_h = 0.23$ cm^2/Vs, respectively, using the relation $dI_{ds} = \mu(V_{ds}/l)(C_g dV_{gs}/l)$. The above μ_e and μ_h do not necessarily represent the crystal quality of the nanowires since the subthreshold gradient $S = (d\log I_{ds}/dV_{gs})^{-1}$ is 170 mV/decade and 130 mV/decade for the *n*- and *p*-channel VSG-FETs, respectively. They are comparable to those of carbon nanotube FETs[28] but larger than that of the state-of-the-art silicon MOSFETs, and this indicates relevant contact effects on μ_e and μ_h. We note that μ_e and μ_h are comparable to those in traditional microscale

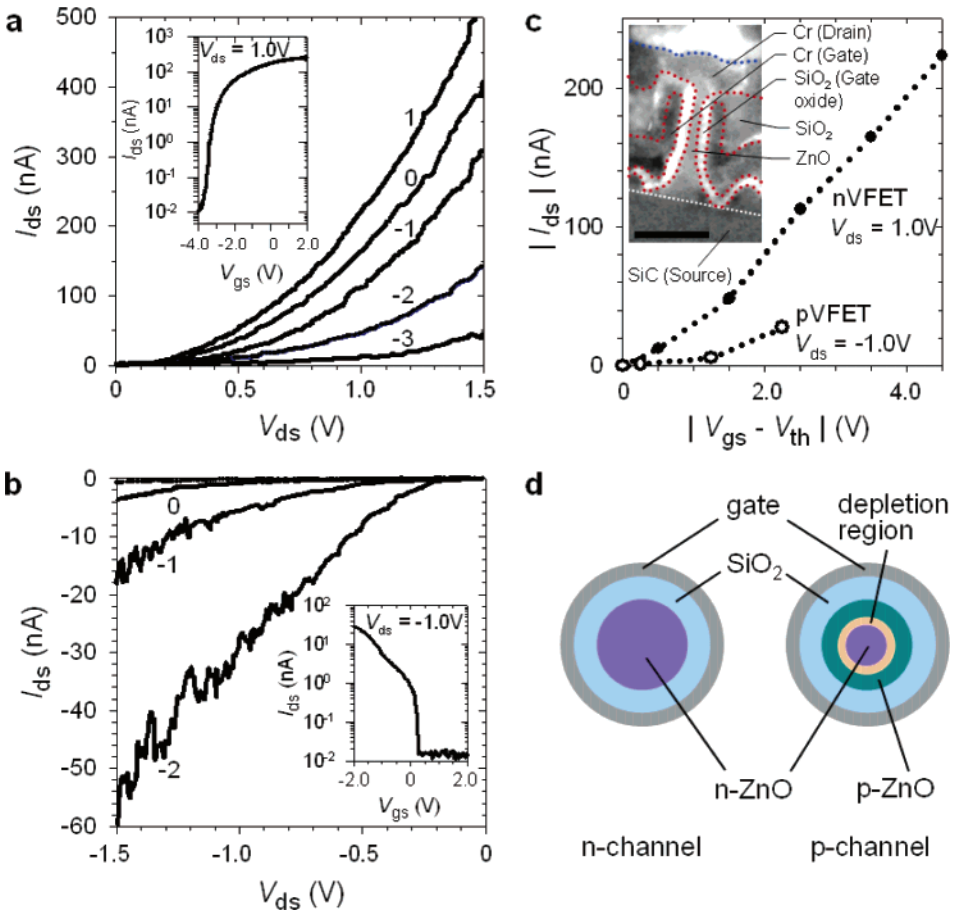

Figure 4. Device characteristics of ZnO nanowire-based *n*- and *p*-VSG-FETs. (a) I_{ds} vs V_{ds} characteristics for different V_{gs} of a *n*-VSG-FET. The inset shows its transfer characteristics at $V_{ds} = 1.0$ V. (b) I_{ds} vs V_{ds} characteristics for different V_{gs} of a *p*-VSG-FET. The inset shows its transfer characteristics at $V_{ds} = -1.0$ V. (c) $|I_{ds}|$ vs $|V_{gs} - V_{th}|$ plots for both VSG-FETs. The inset shows a FE-SEM cross-sectional image of a VSG-FET with a channel length ~200 nm. Scale bar: 200 nm. (d) Cross-sectional schematics of *n*- (left) and *p*- (right) channels of VSG-FETs where the top drain and bottom source electrodes are deliberately not shown. The dimensions of the various components are not drawn to scale.

ZnO-based thin-film transistors.[29,30] In our experiment, the device geometry is not optimized. Further enhancement in device performance, i.e., a higher on-to-off current ratio, higher transconductance, and a lower *S*, can be achieved by using a high-k dielectric material with reduced thickness, improving the channel transport and the source/drain contacts.

In conclusion, we have demonstrated the importance of substrate engineering to grow highly regular and vertically aligned nanowire arrays, and unique direct integration of the nanowires using current semiconductor processing technology, bridging the gap between microtechnology and nanotechnology. Our device fabrication approach has allowed a lithography-free means of defining the vertical channel length by CMP and reduced the footprint of the devices since the drain, source, and channel are stacked on top of each other vertically. The VSG-FETs can be fabricated with cell size featuring at least a 10% smaller footprint than the current state-of-the-art MOSFET,[8] with the potential of achieving tera-level ultrahigh packing density and radiation-hard electronic devices. Though this work involves ZnO nanowires, current work with silicon and germanium nanowires appears promising.

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Supporting Information Available: Generic platform configuration and various applications (Figure 1S). This material is available free of charge via the Internet at http://pubs.acs.org.

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(27) In the *p*-VSG-FET, the source is p^+-SiC. If the channel is *n*-type, the source-channel junction is in the *p*−*n forward* direction with negative V_{ds} while the channel-drain junction is in the Schottky *reverse* direction. This would result in very little conduction. If the channel is *p*-type, the source-channel junction is ohmic, and the channel-drain junction is in the Schottky *forward* direction, resulting in substantial conduction. Thus, we should expect significant contribution of conduction from the *p*-portion, but negligible from the *n*-portion of the *p*-VSG-FET, as shown schematically in Figure 4d.
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