Resume

Ramesh Krishna Jayaraman

Current Status

PhD Student **September 2015 - Present**
Computer Engineering, UC Santa Cruz

Research Interests

My major area of interest lies in **High Performance Computing Architectures** and **Parallel Programming Models.**

- Heterogeneous Many Core Architectures
- Algorithms and Parallel Programming
- Parallel Programming Models
- Compiler Design
- Operating Systems

Research Projects Involved

WARFT Parallel Programming Language (WPPL) and Compiler
Currently working on developing an application and architecture aware parallel programming model to bridge the gap between the application, programming language and the underlying architecture. Developing a compiler to support the proposed programming model.

WARFT Network Processor
Part of the team that developed a customizable network processor to handle data packets in a cluster network dynamically, by establishing a critical path, taking into account traffic and performance aspects of the network.

Algorithm Level Functional Units
Part of team that worked in designing Higher Level functional units as a part of heterogeneous multicores which can lead to the inception of the SuperComputer On Chip (SCOC) IP core paradigm for designing high performance and low power supercomputing clusters.

Compiler on Silicon
Part of the team which developed a model for a table based, dynamic, hard wired compiler cum scheduler. Defined scheduling heuristics to accelerate code generation process.

On Core Network
Part of the team that developed a scalable and reconfigurable Multi-stage Interconnection Network (Omega, Banyan, Benes and Clos) for optimizing performance of heterogeneous multi-cores through WIMAC simulations.

WIMAC(WARFT India Many Core) Simulator
WARFT's initiative to develop a heterogeneous multi-core architecture simulatior to capture the architectural dynamics with cycle accuracy by simulating the integrated working of node architecture, dynamic hardware based compiler cum scheduler, heuristics driven memory subsystems and an integrated optimization engine which are developed based on CUBEMACH, a design paradigm for future generation supercomputing clusters.

UG Thesis (Anna University)

A Heuristic Based Approach to Optimise Algorithms

The objective of this project is to come up with a heuristic based approach to use probabilistic and statistical analysis for the purpose of optimisation of data intensive algorithms. This allows for better results and faster execution times for data intensive algorithms when working on similar data sets.

Research Thesis at WARFT

Application and Architecture Aware Parallel Programming Model

Currently working on the developing of a user-friendly low level parallel programming model and associated constructs which are based on the application for which the programming model is to be used and the architecture on which the application is to be run, for optimal use of the hardware leading to power-performance efficiency. The thesis also involves development of a suitable compiler for the proposed programming model.

Coding Experience

WIMAC - Warft India Many Core Simulator

- Member of the development team of node level, cycle accurate heterogeneous many core simulator based on CUBEMACH design paradigm.
- Upgraded the simulator with new architectural changes (Version 3.1) and iteratively tested the older versions and fixed bugs.

Network Processor Simulator

- Currently working as a part of the development team of Network Processor Simulator, to facilitate high speed data transfer across nodes in a heterogeneous multi-core cluster system.

WARFT Parallel Programming Language and Compiler

- Currently working as a part of the development team of WARFT Parallel Programming Language and Compiler, an application and architecture aware parallel programming constructs and its associated compiler.

Other Coding experiences

- Proficient in programming languages like **C and C++** and familiar with **Python**.
- Editing and publishing of research material drove me to use typesetting tools such as **LaTeX, Microsoft Word** and graph plotting tools like **GNU Plot**.
- Familiar with **CUDA, a parallel programming and computing platform, developed by NVIDIA.**
- Familiar with **Message Passing Interface (MPI)** and **Open Multi-Processing (OpenMP)**
- My Bachelor of Engineering program gave me a wide exposure to various programming languages like **JAVA, JavaScript, HTML5, XML, pHp, Bash Shell Scripting** and syntaxes present in **SQL**.
- Familiar with **Chapel, a parallel programming language developed by CRAY Inc.**
- Experience in working with **Rational Rose.**
- Familiar with **8051, 8085 and 8086 assembly programming**.
- Experienced in working with image processing tools like **Adobe Flash**, **Corel Draw** and **Adobe Photoshop**.