Rafael T. Possignolo

PhD Candidate

email: check site
https://users.soe.ucsc.edu/~rafaeltp

Current Position

I am a PhD candidate working on the intersection between computer architecture and design automation. My main research interest is improving the productivity of hardware designers, for that goal, I am currently working on: automated design pipelining, fast and interactive synthesis methods.

Education

2012-present	**Ph.D. in Computer Engineering**
Research	Live synthesis flow and novel techniques for automated pipeline optimizations University of California, Santa Cruz
2011-2012	**M.Sc. in Electrical Engineering**
Thesis	Design of a quantum co-processor for cryptography algorithms optimization Escola Politéctina, University of Sao Paulo
2009-2010	**M.Sc. in Information, Systems and Technology**
Thesis	Modeling and Optimization of a performance predictive and automatic exploration flow on multi FPGA platform Ecole Nationale Superieure des Techniques Avancées, joint program with Université Paris Sud XI (Orsay), France
2008-2010	**Diplôme d'Ingénieur** Ecole Nationale Superieure des Techniques Avancées, France (Double Degree)
2005-2010	**Computer Engineering Degree** Escola Politécnica, University of São Paulo, Brazil

Work Experience

Summer 2013 — PhD Level Intern at Xilinx, San Jose, CA
Modeled, created automation tools and evaluated FPGA interconnect capacities. Proposed a soft Network-on-Chip communication paradigm to connect IP blocks in FPGAs (Verilog and TCL).

Summer 2012 — PhD Level Intern at Xilinx, San Jose, CA
Designed, developed and tested a pipeline analysis tool for synchronous RTL systems (C++ with TCL interface). Tool currently ships to customers.

Mar - Aug 2010 — MSc. Level Intern at EVE Engineering (currently part of Synopsys), Paris, France
Designed and implemented a NoC based many-core (1000+) over a multi-FPGA platform. Tested and debugged with simulation tools and during emulation on the multi-FPGA platform.

May - Aug 2009 — Research Intern at ENSTA, Paris, France
Implemented, simulated and tested an optimal Neural Network on embedded systems for long and noisy time series (VHDL and C)

Technical Skills

Languages:	Programming (C/C++, Java, Ruby), HDL (Verilog, VHDL, SystemC, Chisel), Typeset (HTML, Markdown, TEX)
Scripting:	Ruby, BASH, SED, AWK, TCL, Python
Tools:	Design (VCS, Synopsys DC/ICC, Vivado, ModelSim, Cadence Virtuoso, HSPICE, PyCells, FreePDK), Version Control (git, svn, p4), General (MATLAB, Octave, Simulink, LabVIEW, R, gnuplot)
Simulators:	ESESC, CACTI, McPAT, SimpleScalar
Equipments:	Arduino, Xilinx FPGAs and Boards, Zebu Platform, Oscilloscope

Languages

Fluent: Portuguese, English, French
Some Knowledge: Spanish, German

Honors and Awards

Fall 2016	Invitation to write a book chapter based on my current research (currently under edition by Springer)
Fall 2012	UC Regents' Fellowship
Winter 2012	Miguel Velez Award for South America Students with good standing
2008 - 2010	Eiffel Excellence Scholarship Award for top international students

Journal Articles

[1] Ehsan K. Ardestani et al. "Managing Mismatches in Voltage Stacking with CoreUnfolding". In: *ACM Trans. Archit. Code Optim.* 12.4 (Nov. 2015), 43:1–43:26. ISSN: 1544-3566. DOI: 10.1145/2835178.

[2] Rafael T. Possignolo, Cintia B. Margi, and Paulo S. L. M. Barreto. "Quantum-assisted QD-CFS signatures". In: *Journal of Computer and System Sciences* 81.2 (2015), pp. 458 –467. ISSN: 0022-0000. DOI: http://dx.doi.org/10.1016/j.jcss.2014.10.003.

Conference and Workshop Papers

[3] Elnaz Ebrahimi, Rafael T. Possignolo, and Jose Renau. "Level Shifter Design for Voltage Stacking". In: *Circuits and Systems (ISCAS), Proceedings of the 2017 IEEE International Symposium on*. 2017.

[4] Rafael T. Possignolo and Jose Renau. "LiveSynth: Towards an Interactive Synthesis Flow". In: *Design Automation Conference (DAC'17), Proceedings of the 2017*. 2017.

[5] Elnaz Ebrahimi, Rafael T. Possignolo, and Jose Renau. "SRAM Voltage Stacking". In: *Circuits and Systems (ISCAS), Proceedings of the 2016 IEEE International Symposium on*. 2016.

[6] Ilya Ganusov et al. "Automated Extra Pipeline Analysis of Applications Mapped to Xilinx UltraScale+ FPGAs". In: *Field Programmable Logic and Applications (FPL), Proceedings of the 26th Conference on*. 2016.

[7] Rafael T. Possignolo et al. "FluidPipelines: Elastic Circuitry meets Out-of-Order Execution". In: *Computer Design (ICCD), Proceedings of the 34th International Conference on*. 2016.

[8] Rafael T. Possignolo et al. "FluidPipelines: Elastic Circuitry without Throughput Penalty". In: *Logic Synthesis (IWLS), Proceedings of the 2016 International Workshop on*. 2016.

[9] Rafael T. Possignolo and Cintia B. Margi. "A Quantum-classical Hybrid Architecture for Security Algorithms Acceleration". In: *Trust, Security and Privacy in Computing and Communications (TrustCom), 2012 IEEE 11th International Conference on*. 2012, pp. 1032–1037. DOI: 10.1109/TrustCom.2012.49.

[10] Laio B. Vilas-Boas et al. "Performance evaluation of QoS in wireless networks using IEEE 802.11 e". In: *Telecomunicações (SBrT'12), Proceedings of the XXX Simpósio Brasileiro de*. 2012.

[11] Rafael T. Possignolo and Omar Hammami. "Performance evaluation of hybrid ANN based time series prediction on embedded processor". In: *Latin American Symposium on Circuits and Systems (LASCAS), Proceedings of the 2010 First IEEE*. 2010, pp. 204–207. DOI: 10.1109/LASCAS.2010.7410246.

[12] Rafael T. Possignolo and Omar Hammami. "Optimized joint NARX ANN - embedded processor design methodology". In: *Electronics, Circuits, and Systems, 2009. ICECS 2009. 16th IEEE International Conference on*. 2009, pp. 499–502. DOI: 10.1109/ICECS.2009.5410883.

Poster Presentations

[13] Rafael T. Possignolo and Jose Renau. *LiveSynth: Towards an Interactive Synthesis Flow*. Poster presented at the 28th HotChips: A symposium for High Performance Chips. 2016.

[14] Rafael T. Possignolo, Elanz Ebrahimi, and Jose Renau. *ReCycling of Elastic Systems without Throughput Penalty*. Work-in-Progress Poster presented at the 52th Annual Design Automation Conference, DAC'15, June 7–11, San Francisco, CA. 2015.

[15] Rafael T. Possignolo et al. *GPU NTC Process Variation Compensation with Voltage Stacking*. Work-in-Progress Poster presented at the 2015 Parallel Architectures and Compilation Techniques (PACT), International Conference on. 2015.

[16] Rafael T. Possignolo et al. *Quantum Assisted CFS Signatures*. Poster presented at the III Quantum Information and Computation School, QIC'2011, August, 2011, Paraty, RJ, Brazil. 2011.