S2014, BME 101L Applied Circuits Lab 9 addendum: open-collector outputs in class-D power amplifier

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1 LM2903 comparators

Your FET output stage needs to have gate voltages that make a large voltage change rapidly, but our MCP6004 op amps are not capable of doing that. Not only are they limited to a maximum voltage swing of about 6V, they have a designed-in speed limitation: a slew rate of 0.6V/μs, so it would take them 10μs to do even their full 6V swing.

Because of these limitations of the op amp, I've provided another chip in your parts kit: the LM2903 dual comparator chip. The comparator chip can have a 30V difference between the top voltage and bottom voltage, so there is no problem powering it from your dual-rail supply, which has at most an 18V difference.

One warning (a mistake I made in 2013): be sure that your inputs to the LM2903 (coming from the preamplifier and the triangle-wave generator) remain between the power rails of the LM2903. I've not damaged an LM2903 this way (yet), but they don't work properly outside their power rails. I think I did damage the tlc3702 comparators by having an input that went too far below the bottom rail.

The LM2903 has a different sort of output than the op-amps and Schmitt triggers you've used so far—an open-collector output. When the positive input is higher than the negative input, there is essentially no current through the output, but when the positive input is lower than the negative input, the output can sink up to about 7.5mA. If you look at the data sheet, you see a couple of different numbers $V_{OL} < 400mV$ at $I_{OL} = 4mA$ and $I_{OL} > 6mA$ at $V_{OL} = 1.5V$.

Note: V_{OL} is "voltage output low"—the voltage that you get when trying to drive the output down. V_{OH} is "voltage output high", the voltage when the output is high. You have to be careful when using these numbers to keep track of what the voltage is referenced to (the "ground node"? the lower power rail?) Remember that a voltage is always a difference between two nodes, even when only one node seems to be referred to. The numbers for V_{OL} on the data sheet are referenced to the V_- power supply input of the LM2903 chip.

To get the output to ever move away from the lower power rail, you need a pull-up resistor to provide current when the LM2903 output is off and pull the output up (See Figure 1). Sizing that pull-up is a design task—let's look at the constraints on it. The LM2903 and pull-up resistor need to drive the gates of the FETs high and low (enough to turn the FETs fully off) rapidly. The gates of FETs are essentially capacitors. You can look up the input capacitance on the data sheets for the FETs, though the gate-charge model provides a better calculation of the time it takes to turn on or off the transistors.

To choose values for the pull-up resistors, we need to know how the output of the LM2903 behaves. When the output is supposed to be high, there is no current through the LM2903 output, and the gate capacitance is charged through the pull-up resistor to whatever voltage the other end of the resistor is connected to. That is, the output-high voltage V_{OH} is just whatever the resistor is connected to. When the output is supposed to be low, the output-low voltage V_{OL} depends on the current through the LM2903 output transistor and the resulting IR drop across the pull-up resistor: $V_{OL} = V_{OH} - I_{sat}R$.

If you make the pull-up resistor very large, then a low output will be discharging the FET gates rapidly with about 10mA of current through the LM2903 outputs, but a high output will charge the FET gates very slowly through the large pull-up resistor. That is, a large resistor will turn the nFET on slowly but off quickly, but will turn the pFET off slowly and on quickly.

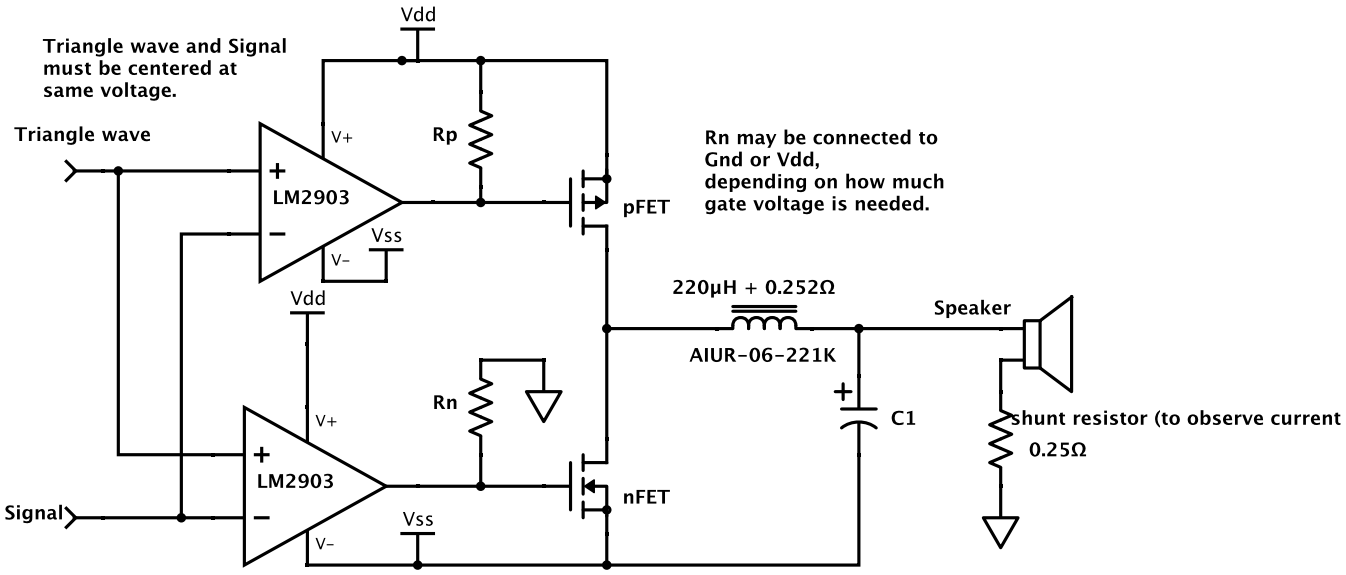

Figure 1: By having separate control signals for the gates of the nFET and pFET, we can arrange the signals to the gates so that the FETs are not simultaneously on. The basic idea is to make sure that the FETs are turned off quickly, even at the cost of turning on more slowly. (Note: the shunt resistor in series with the loudspeaker is optional, but useful if you want to observe or measure the current through the loudspeaker.)

If you make the pull-up resistor very small, then the open-collector current through the LM2903 to the lower voltage rail may not provide enough voltage drop across the resistor, and you might not be able to get a low enough output voltage to turn off the nFET fully. That would result in a lot of wasted power through the cMOS output stage and overheating the FETs. A small resistor will make the nFET turn on quickly and off slowly, but the pFET turn off quickly and on slowly.

The optimal design for the nFET pullup would be a small enough value for a small RC charging time for a high output and yet large enough to ensure that the low output shuts off the nFET quickly. Similarly the pFET pullup should be small enough to turn the pFET off quickly, but large enough that the pFET is turned on fully when needed.

The spec sheets for the LM2903 do not give us good values for the output current vs. voltage characteristic, so I tried measuring it with the same techniques we used earlier in the course to characterize the electret microphone, using load resistors of various sizes (from 1kΩ down to 8.2Ω). The results are shown in Figure 2.

To a first approximation, for V_{OL} higher than 1V above the bottom power rail, we can model the LM2903 as a current source with the saturation current of about $I_{sat} = 18\text{mA}$, and make a Thévenin equivalent for the pull-up resistor, power supply, and LM2903 output transistor.

For each of the FETs, we are interested in the gate-to-source voltage that controls the FET.

nFET driver For the nFET, $V_{GS(nFET)}$ is the gate voltage minus V_{ss}, so the two ports for the Thévenin equivalent are the output of the comparator and V_{ss}.

open-circuit voltage $V_{OC} = (0 - I_{sat}R_n) - V_{ss}$ if the other end of R_n is connected to ground, as shown in Figure 1.

short-circuit current $I_{sc} = -V_{ss}/R_n - I_{sat}$.

So the Thévenin equivalent is a voltage of $-V_{ss} - I_{sat}R_n$ with a resistance of R_n.

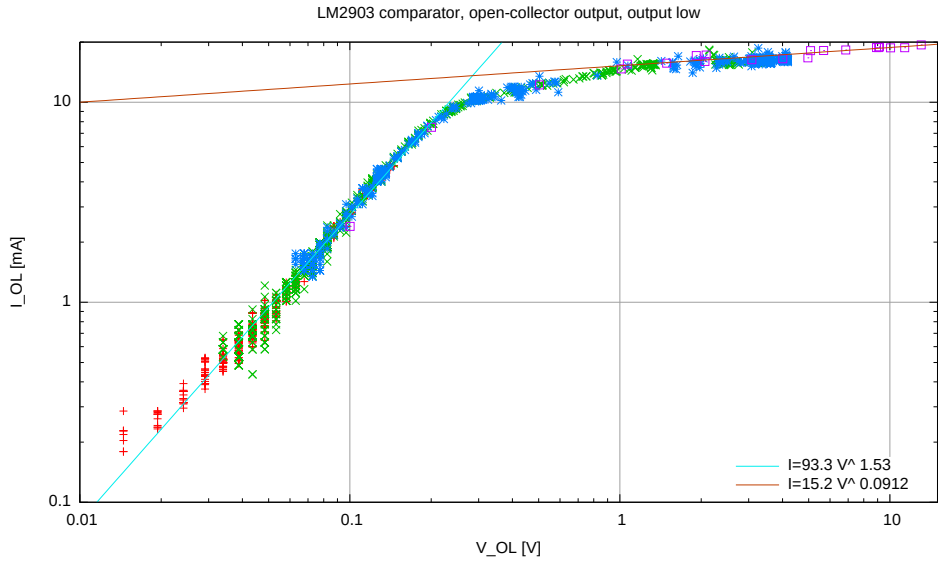

Figure 2: The output of the LM2903 comparator has an output current of around 15mA with $V_{OL} = 1$ and a saturation current around 18mA, even for $V_{OL} = 13v$, which is as high as I could measure at home. Note that I measured around 14–16mA at 1.5V, much more than the minimum spec of 6mA. It is often the case that minimum specs are much more conservative than typical values, to account for variation due to temperature, aging of parts, or variation in the manufacturing. The saturation current curve seems to depend somewhat on the voltage supplied to the LM2903 V_{CC} input, increasing somewhat with higher V_{CC}, but I did not investigate this carefully, due to lack of time.

If we use a ±7v power supply $V_{ss} = -7$v) and $R_n = 100\Omega$ connected to ground, then $V_{GS(nFET)} = (0v - 18\text{mA}100\Omega) - (-7\text{v}) = 5.2\text{v}$. That is way too high a voltage to turn off the nFET, so a 100Ω resistor is clearly far too small a resistance for R_n at that voltage.

Prelab: Compute the minimum resistor size that you can use to ensure that the nFET is completely turned off. Note that this means getting $V_{GS(nFET)} < V_{Th(nFET)}$, for the lowest threshold value mentioned on the data sheet. The resistance will depend on your power supply voltage.

pFET driver We can do the same analysis of the comparator driving the pFET, where the gate to source voltage is the gate voltage minus V_{dd} (which gives a $V_{GS(pFET)} \leq 0$):

open-circuit voltage $V_{OC} = (V_{dd} - I_{sat}R_p) - V_{dd}$

short-circuit current $I_{sc} = -I_{sat}$.

So the Thévenin equivalent is a voltage of $-I_{sat}R_p$ with a resistance of R_p.

If we use a ±7v power supply and $R_p = 100\Omega$, then we get $V_{GS(pFET)} = -18\text{mA}100\Omega = -1.8\text{v}$, which is almost, but not quite enough to turn on the pFET. So 100Ωis too small for R_p at this voltage.

Prelab: Compute the minimum resistor size that you can use to ensure that the pFET is completely turned on. Note that this means getting $V_{GS(pFET)} < V_{Th(pFET)}$ (both are negative numbers), for the most negative threshold value mentioned on the data sheet.

Note that for both pulling up (when the comparator output is floating) and pulling down, the Thévenin equivalent resistance is the pullup resistance R, so we can figure out rise and fall times by how many RC time constants it takes to reach a certain voltage.

If we start at V_0 and charge or discharge towards an endpoint of V_∞, then the charging curve is approximately $V(t) = V_\infty + (V_0 - V\infty)e^{-t/(RC)}$ and the time it takes to reach $V(t)$ is

$$t = RC \ln \frac{V_0 - V_\infty}{V(t) - V_\infty} \ . \tag{1}$$

This formula is a handy one for estimating how long it takes an FET to be turned off or on, though it is a rather crude approximation, since the gate capacitance is not really constant.

In sizing the pull-up resistors for the comparator outputs, you'll have the following considerations:

- The comparator driving the nFET must have a low enough output voltage when the output is supposed to be low that the nFET is turned completely off ($V_{GS(nFET)} < V_{Tn} \approx 1.8$v This requires having a large enough pull-up resistor R_n that the voltage drop IR_n across the resistor is big enough. If the power voltages are increased, a larger IR drop is needed to keep the low output voltage below the threshold voltage above the lower power rail.

- The comparator driving the nFET must have a high enough output voltage when the output is supposed to be high (V_{OH}) to turn on the nFET This is trivial to arrange, as long as the voltages on the power rails are big enough, as the V_{OH} of the pulled-up open-collector output is whatever the other end of the pullup resistor is connected to.

- The comparator driving the pFET must have a high enough V_{OH} that the pFET is turned completely off. This is also trivial to arrange, since there is no DC current flow, and V_{OH} is the upper power rail.

- The comparator driving the pFET must have a low enough V_{OL} that the pFET is turned on, say at least 4V below the upper power rail. This means that the pullup resistor R_p must be large enough that the IR_p drop is at least 4V, and preferably more. That is $I_{sat}R_p > 4$V.

- To make sure that we are getting fast rise times compared to our PWM frequency, we want $R_nC_n \ll T_{PWM}$ and $R_pC_p \ll T_{PWM}$, where T_{PWM} is the period of the triangle wave input to the comparator.

- We are interested in how long it takes the nFET and the pFET to turn on and off, and we can use the charging/discharging formula in Equation 1, paying attention to what voltage we start at, what voltage we end at, and what threshold voltage we are interested in determining the time to reach.

  The algebra gets a bit tedious if you try to work this for different power supply voltages and resistors, but it is easy to write a gnuplot script and plot the time to turn on or off the transistors times for various parameter values (see Figures **??**, **??**, and **??**).

  Note that you'll want R_p to be fairly small, to turn the pFET off quickly (but not so small that the pFET is not turned on when it is supposed to be) and a fairly large R_n so that the nFET is turned off quickly when it is supposed to be, but not so large that the nFET turn on time is more than about a microsecond.

  We have a problem: the pFET turns on quite quickly for any reasonable value of R_p and the nFET turns off rather slowly. That means that there will be a short time when both the nFET and the pFET are on at the same time. This "shoot-through" current can be quite large, so we need to ensure that it doesn't last long–no more than about 5% of the total PWM period

So we have several constraints on R_n and R_p, some of which depend on the gate capacitances and PWM frequency, some of which depend on the power supply voltages, and some of which depend on the maximum current through the LM2903 output transistors.

```
set ylabel "Charge/discharge time [microsec]"
set xlabel "Pull-up resistance [ohm]"
set samples 20000

# time in microseconds to charge C in F through R in ohms
# from V0 to Vth when the target voltage as t->infinity is Vinf
charge_time(r,c,V0,Vinf,Vth) = 1e6* r*c* log( (V0-Vinf) / (Vth-Vinf))

set xrange[100:2000]
set yrange [0.01:10]
set logscale xy
set key top left

Vsupply=9 # power supply is +- Vsupply (V)
Isat = 0.018    # saturation current of open-collector comparator (A)

# Threshold voltage(s) and gate capacitance for AOI518 nFET
Vntsmall=1.8 # (V)
Vntbig=2.6 # (V)
Cn=1187e-12 # (F)

# Threshold voltage(s) and gate capacitance for IRFU9024NPbF pFET
Vptbig=-4.0 # (V)
Vptsmall=-2.0 # (V)
Cp=350e-12 #(F)

set title \
 sprintf("LM2903, +-%.3gV power, on/off times for nFET, Isat=%3gmA",\
         Vsupply,Isat*1e3)

plot \
     charge_time(x,Cn,Vsupply,Vsupply-x*Isat,Vntsmall) \
      title sprintf("nFET off V_T=%.2f Rn to gnd", Vntsmall), \
     charge_time(x,Cn,Vsupply,Vsupply-x*Isat,Vntbig) \
      title sprintf("nFET off V_T=%.2f Rn to gnd", Vntbig), \
     charge_time(x,Cn,Vsupply-x*Isat,Vsupply,Vntbig) \
      title sprintf("nFET on V_T=%.2f Rn to gnd", Vntbig), \
     charge_time(x,Cn,Vsupply-x*Isat,Vsupply,Vntsmall) \
      title sprintf("nFET on V_T=%.2f Rn to gnd", Vntsmall)
```

Figure 3: Gnuplot script to plot the time to charge or discharge an nFET gate to a particular threshold. The script is available at `http://users.soe.ucsc.edu/~karplus/bme101/s14/nfet-times.gnuplot`. A similar script for pFETs is available at `http://users.soe.ucsc.edu/~karplus/bme101/s14/pfet-times.gnuplot`. You will have to adjust the supply voltage and decide which values to use for the threshold voltages. The results of running the script with the parameters shown here is in Figure 4.

Prelab: It is a good idea to write down all the constraints, to see if there are any reasonable solutions for R_n and R_p. There is a fairly wide range of values possible for the R_n and R_p values, based on these constraints, but you probably want to use the smallest values that are consistent with the constraints, in order to keep the rise and fall times as short as possible.

After choosing your PWM frequency and your power-supply voltage, go through the constraints on R_n and R_p to see if you can come up with resistances that meet all the constraints. If you pick too high a PWM frequency or too large a power-supply voltage, there may not be values that work.

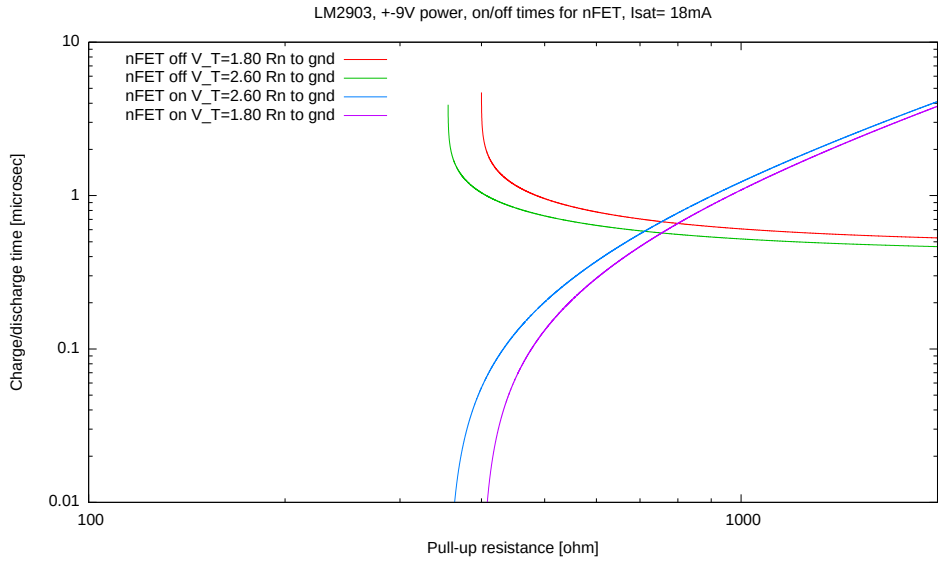

Figure 4: The result of running the gnuplot script of Figure 3. The resistance values where the times go asymptotically to ∞ are the absolute minimum values for R_n. Note that you don't have a choice of threshold voltages, so you need to design for the worst case. Also note that even very large resistors won't give you a very fast turn-off time—even without a pullup resistor to fight, it takes a while for a current of I_{sat} to drain the charge off the nFET gate.

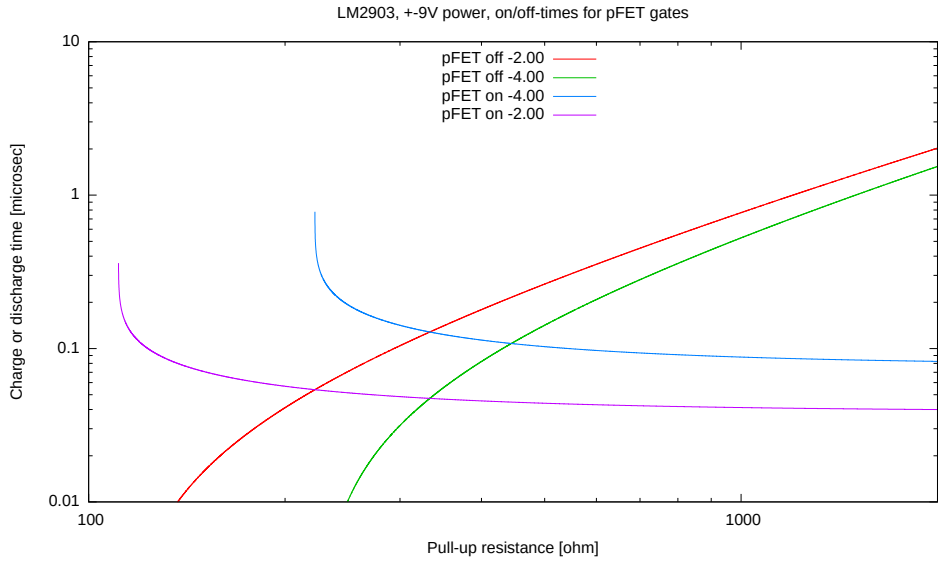

Figure 5: The result of running a similar script for the pFET rather than the nFET. The resistance values where the times go asymptotically to ∞ are the absolute minimum values for R_p. Note that you don't have a choice of threshold voltages, so you need to design for the worst case.