Jishen Zhao

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Assistant Professor, Computer Engineering
University of California at Santa Cruz

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Education

2009 - 2014 Ph.D. in Computer Science and Engineering, Pennsylvania State University
2003 - 2008 M.Eng. in Electrical Engineering, Zhejiang University
1999 - 2003 B.Eng. in Electrical Engineering, Zhejiang University

Research Interests

A broad range of computer system and architecture with an emphasis on memory and storage systems, high-performance computing, and energy efficiency. Electronics design automation and VLSI design for three-dimensional integrated circuits and nonvolatile memories.

Professional Experience

2015 - present **University of California at Santa Cruz**
Assistant Professor in Computer Engineering Department

2014 - 2015 **Hewlett-Packard Labs**
Research Scientist at Systems Research Lab

2012 - 2013 **Hewlett-Packard Labs**
Research Associate at Intelligent Infrastructure Lab

Honors & Awards

2017 NSF CAREER Award
2013 Best Paper Honorable Mention Award at MICRO, 2013
2006 National champion of Small Size League, RoboCup China 2006
2006 Final Eight of Small Size League, RoboCup International 2006 (Bremen, Germany)

Books

[1] Yuan Xie and Jishen Zhao. Die-stacking architecture. *Synthesis Lectures on Computer Architecture. Morgan & Claypool Publishers*, 2015.

Publications

[1] Hengyu Zhao*, Linuo Xue*, Ping Chi, and Jishen Zhao. Approximate image storage with multi-level cell stt-mram main memory. In *Proceedings of the International Conference On Computer Aided Design (ICCAD)*, 2017. (The first two authors contribute equally).

[2] Liang Chang, Zhaohao Wang, Alvin Oliver Glova, Jishen Zhao, Youguang Zhang, Yuan Xie, and Weisheng Zhao. PRESCOTT: Preset-based cross-point architecture for spin-orbit-torque magnetic random access memory. In *Proceedings of the International Conference On Computer Aided Design (ICCAD)*, 2017.

[3] Chun-Hao Lai, Jishen Zhao, and Chia-Lin Yang. Leave the cache hierarchy operation as it is: A new persistent memory accelerating approach. In *Proceedings of of the 54th Design Automation Conference (DAC)*, 2017. Acceptance Rate: 161/676=23.8%.

[4] Jia Zhan, Itir Akgun, Jishen Zhao, Al Davis, Paolo Faraboschi, Yuangang Wang, and Yuan Xie. A unified memory network architecture for in-memory computing in commodity servers. In *Proceedings of the International Symposium on Microarchitecture (MICRO)*, 2016. Acceptance Rate: 61/283=21.6%.

[5] Yuxiong Zhu, Borui Wang, Dong Li, and Jishen Zhao. Integrated thermal analysis for processing in die-stacking memory. In *Proceedings of International Symposium on Memory Systems (MEMSYS)*, 2016.

[6] Borui Wang, Martin Torres, Dong Li, Jishen Zhao, and Florin Rusu. Performance implications of processing-in-memory designs on data-intensive applications. In *5th Workshop on Heterogeneous and Unconventional Cluster Architectures and Applications*, 2016.

[7] Ping Chi, Shuangchen Li, Cong Xu, Tao Zhang, Jishen Zhao, Yongpan Liu, Yu Wang, and Yuan Xie. A novel processing-in-memory architecture for neural network computation in reram-based main memory. In *Proceedings of the 43rd International Symposium on Computer Architecture (ISCA)*, 2016. Acceptance Rate: 54/288=18.8%.

[8] Hsiang-Yun Cheng, Jishen Zhao, Jack Sampson, Mary Jane Irwin, Aamer Jaleel, Yu Lu, and Yuan Xie. Lap: Loop-block aware inclusion properties for energy-efficient asymmetric last level caches. In *Proceedings of the 43rd International Symposium on Computer Architecture (ISCA)*, 2016. Acceptance Rate: 54/288=18.8%.

[9] Xiao Liu, Qing Yi, and Jishen Zhao. Using memory-style storage to support fault tolerance in data centers. In *USENIX Workshop on Cool Topics in Sustainable Data Centers (CoolDC)*, 2016.

[10] Shuangchen Li, Cong Xu, Jishen Zhao, Yu Lu, and Yuan Xie. Pinatubo: A processing in non-volatile memory architecture for bulk bitwise operations. In *Proceedings of the 53rd Design Automation Conference (DAC)*, 2016. Acceptance Rate: 152/876=17.4%.

[11] Jishen Zhao, Cong Xu, Tao Zhang, and Yuan Xie. BACH: A bandwidth-aware hybrid cache hierarchy design with nonvolatile memories. *Journal of Computer Science and Technology*, 31:20–35, 2016.

[12] Jinglei Ren, Jishen Zhao, Samira Khan, Jongmoo Choi, Yongwei Wu, and Onur Mutlu. ThyNVM: Enabling software-transparent crash consistency in persistent memory systems. In *International Symposium on Microarchitecture (MICRO)*, 2015. Acceptance Rate: 61/283=21.5%.

[13] Jishen Zhao, Qiaosha Zou, and Yuan Xie. Overview of 3d architecture design opportunities and techniques. *IEEE Design & Test*, 2015.

[14] Jishen Zhao, Sheng Li, Jichuan Chang, John L. Byrne, Laura L. Ramirez, Kevin Lim, Yuan Xie, and Paolo Faraboschi. Buri: Scaling big memory computing with transparent memory expansion. *ACM Transactions on Architecture and Code Optimization (TACO)*, 2015.

[15] Shuangchen Li, Ping Chi, Jishen Zhao, Kwang-Ting Cheng, and Yuan Xie. Leveraging nonvolatility for architecture design with emerging nvm. In *Proceedings of the 4th IEEE Non-Volatile Memory System and Applications Symposium (NVMSA)*, 2015.

[16] Hsiang-Yun Cheng, Jia Zhan, Jishen Zhao, Yuan Xie, Jack Sampson, and Mary Jane Irwin. Core vs. Uncore: The heart of darkness. In *Proceedings of the 52nd Design Automation Conference (DAC)*, 2015. Invited paper.

[17] Ke Chen, Sheng Li, Jung Ho Ahn, Naveen Muralimanohar, Jishen Zhao, Cong Xu, Seongil O, Yuan Xie, Jay B. Brockman, and Norman P. Jouppi. History-assisted adaptive-granularity caches (HAAG$) for high performance 3D DRAM architectures. In *Proceedings of the 29th International Conference on Supercomputing (ICS)*, 2015. Acceptance rate: 40/160=25%.

[18] Jia Zhan, Jin Ouyang, Fen Ge, Jishen Zhao, and Yuan Xie. DimNoC: A dim silicon approach towards power-efficient on-chip network. In *Proceedings of the 52nd Design Automation Conference (DAC)*, 2015. Acceptance Rate: 162/789=20.5%.

[19] Jishen Zhao, Cong Xu, Ping Chi, and Yuan Xie. Memory and storage system design with nonvolatile memory technologies. *IPSJ Transactions on System LSI Design Methodology (TSLDM)*, 8:2–11, 2015. Invited paper.

[20] Jishen Zhao, Onur Mutlu, and Yuan Xie. FIRM: Fair and high-performance memory control for persistent memory systems. In *Proceedings of the 47th International Symposium on Microarchitecture (MICRO-47)*, 2014. Acceptance rate: 53/279=19%.

[21] Jishen Zhao, Sheng Li, Doe Hyun Yoon, Yuan Xie, and Norman P. Jouppi. Kiln: Closing the performance gap between systems with and without persistence support. In *Proceedings of the 46th International Symposium on Microarchitecture (MICRO)*, pages 421–432, 2013. Acceptance rate: 39/239=16%, **Best Paper Honorable Mention**.

[22] Jishen Zhao, Guangyu Sun, Gabriel Loh, and Yuan Xie. Optimizing GPU energy efficiency with 3D die-stacking graphics memory and reconfigurable memory interface. *ACM Transactions on Architecture and Code Optimization (TACO)*, 10(4):24:1–24:25, 2013.

[23] Justin Meza, Yixin Luo, Samira Khan, Jishen Zhao, Yuan Xie, and Onur Mutlu. A case for efficient hardware/software cooperative management of storage and memory. In *Proceedings of the 5th Workshop on Energy-Efficient Design (WEED), held in conjunction with the International Symposium on Computer Architecture (ISCA-40)*, 2013.

[24] Sheng Li, Doe Hyun Yoon, Ke Chen, Jishen Zhao, Jung Ho Ahn, Jay B. Brockman, Yuan Xie, and Norman P. Jouppi. Mage: Adaptive granularity and ecc for resilient and power efficient memory systems. In *Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis (SC)*, pages 33:1–33:11, 2012. Acceptance rate: 100/472=21%.

[25] Jishen Zhao and Yuan Xie. Optimizing bandwidth and power of graphics memory with hybrid memory technologies and adaptive data migration. In *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pages 81–87, 2012. Acceptance rate: 82/338=24%.

[26] Jishen Zhao, Guangyu Sun, Gabriel H. Loh, and Yuan Xie. Energy-efficient GPU design with reconfigurable in-package graphics memory. In *Proceedings of the 18th International Symposium on Low Power Electronics and Design (ISLPED)*, pages 403–408, 2012. Acceptance rate: 34/213=16%.

[27] Jishen Zhao, Cong Xu, and Yuan Xie. Bandwidth-aware reconfigurable cache design with hybrid memory technologies. In *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pages 48–55, 2011. Acceptance rate: 106/349=30%.

[28] Guangyu Sun, Christopher J. Hughes, Changkyu Kim, Jishen Zhao, Cong Xu, Yuan Xie, and Yen-Kuang Chen. Moguls: A model to explore the memory hierarchy for bandwidth improvements. In *Proceedings of the 38th International Symposium on Computer Architecture (ISCA)*, pages 377–388, 2011. Acceptance rate: 40/208=19%.

[29] Jishen Zhao, Xiangyu Dong, and Yuan Xie. An energy-efficient 3D CMP design with fine-grained voltage scaling. In *Proceedings of the IEEE/ACM Design, Automation, and Test in Europe Conference (DATE)*, pages 539–542, 2011.

[30] Xiangyu Dong, Jishen Zhao, and Yuan Xie. Fabrication cost analysis and cost-aware design space exploration for 3D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 29(12):1959–1972, December 2010.

[31] Jing Xie, Jishen Zhao, and Yuan Xie. Architectural benefits and design challenges for three-dimensional integrated circuits. In *Proceedings of the IEEE 11th biennial Asia Pacific Conference on Circuits and Systems (APCCAS)*, pages 540–543, 2010.

[32] Yibo Chen, Jishen Zhao, and Yuan Xie. 3D-nonFAR: Three-dimensional non-volatile FPGA architecture using phase change memory. In *Proceedings of the 16th International Symposium on Low Power Electronics and Design (ISLPED)*, pages 55–60, 2010. Acceptance rate: 52/210=25%.

[33] Jishen Zhao, Xiangyu Dong, and Yuan Xie. Cost-aware three-dimensional (3D) many-core multiprocessor design. In *Proceedings of the 47th Design Automation Conference (DAC)*, pages 126–131, 2010. Acceptance rate: 148/607=24%.

Patents

[P1] Douglas L Voigt, Charles B Morrey, Jishen Zhao, Dhruva Chakrabarti, and Joseph E Foster. Persistent memory versioning and merging. *WO2016160035*

[P2] Stanko Novakovic, Paolo Faraboschi, Kimberly Keeton, Jishen Zhao, Robert Schreiber. Responsive server identification among multiple data servers linked to a shared memory. *WO2016137496.*

[P3] Rajeev Balasubramonian, Naveen Muralimanohar, Gregg B. Lesartre, Paolo Faraboschi, Jishen Zhao. Data write to subset of memory devices. *WO2016144291.*

[P4] Sheng Li, Jishen Zhao, Kevin T Lim, and Paolo Faraboschi. Node-based computing devices with virtual circuits. *WO2016014043.*

[P5] Sheng Li, Paolo Faraboschi, Kevin T Lim, Jishen Zhao. Node-based computing devices with protocol-based priority. *WO2016014044.*

[P6] Sheng Li, Jichuan Chang, and Jishen Zhao. Dynamic memory expansion by data compression. *WO2015142341*.

[P7] Sheng Li, Jishen Zhao, Jichuan Chang, Parthasarathy Ranganathan, Alistair Veitch, Kevin T. Lim, and Mark Lillibridge. Atomically Committing Write Requests *US Patent 20160342351*

[P8] Sheng Li, Jishen Zhao, Jichuan Chang, Mapping virtual memory pages to physical memory pages. *US Patent 20160267015*.

[P9] Doe Hyun Yoon, Sheng Li, Jishen Zhao, and Norman P. Jouppi. Multiversioned nonvolatile memory hierarchy for persistent memory. *US Patent 20160034225*.

Invited Presentations, Seminars, and Others

[1] Workload Characterization and Hardware Support for Persistence, *Ulsan National Institute of Science and Technology, Ulsan, Korea, Jul. 2016*.

[2] Workload Characterization and Hardware Support for Persistence, *International Forum on MPSoC for Software-defined Hardware, Nara, Japan, Jul. 2016*.

[3] Persistent memory architecture research at UCSC, *SK Hynix, San Jose, California, June 2016*.

[4] Re-architecting the Memory-Storage Stack with NVRAMs, *University of California, Merced, Aug. 2015*.

[5] Memory persistence: a new dimension in memory system design, *SanDisk TechCon'15, Milpitas, California, Jul. 2015*.

[6] Memory Persistence: A New Dimension in Memory System Design, *International Forum on MPSoC for Software-defined Hardware, Santa Barbara, California, Jul. 2015*.

[7] Rethinking Memory System Organization with Emerging Technologies, *Northwestern University, Mar. 2014*.

[8] Rethinking Memory System Organization with Emerging Technologies, *University of California at Santa Cruz, Feb. 2014*.

[9] Rethinking Memory System Organization with NVRAMs, *HP Labs, Sep. 2013*.

[10] Energy-efficient Reconfigurable Memory Hierarchy Design with Emerging Technologies, *ACM Student Research Competition at ICCAD, 2013*

[11] Bandwidth-Aware Reconfigurable Cache Hierarchy Design with Hybrid Memory Technologies, *First CRA-W/CDC Workshop on Diversity in Design Automation and Test (WD2AT), May 2011*.

[12] Reconfigurable Energy-Efficient 3D Stacked Chip-Multiprocessor Design, *SRC TECHCON, Sep. 2010*.

Professional Services and Activities

Conference/Workshop/Session Organizer:

1. Publicity co-chair, International Symposium on High-Performance Computer Architecture (HPCA), 2018
2. Publicity co-chair, International Workshop of Software-Defined Data Communications and Storage (SD-DCS), Co-located with ASPLOS 2017
3. DAC'16 special session "Winning the Memory Challenge: Which Non-volatile Memory Technology Will Rise Above", June, 2016
4. Finance co-chair, International Forum on MPSoC for Software-defined Hardware, 2015

Technical Program Chair, Track Chair/Co-chair:

1. TPC Track Co-chair, Architecture Track, IEEE International Conference on Networking, Architecture, and Storage (NAS), 2016

Program Committee Member in Conferences:

1. IEEE International Symposium on Workload Characterization (IISWC), 2017
2. Architecture track, IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2017
3. ACM/IEEE Design Automation Conference (DAC), 2016, 2017
4. International Conference on Massive Storage Systems and Technology (MSST), 2016, 2017
5. International Symposium on Low Power Electronics and Design (ISLPED), 2015 - 2017
6. International Symposium on Memory Systems (MEMSYS), 2017
7. ACM International Conference on Computing Frontiers (CF), 2015 - 2017
8. International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2015 - 2017
9. IEEE Non-Volatile Memory System and Applications Symposium (NVMSA), 2015 - 2017
10. Great Lakes Symposium on VLSI (GLSVLSI), 2014 - 2017
11. International Conference on Networking, Architecture, and Storage (NAS), Storage track, 2017
12. International Conference for High Performance Computing, Networking, Storage and Analysis (SC), 2016
13. International Conference on Super Computing (ICS), 2016
14. IEEE International System-on-Chip Conference (SOCC), 2015
15. ESWeek Internet-of-Things Symposium (IoT), 2015
16. IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2015 - 2016
17. Workshop on Architectures and Systems for Big Data (ASBD), 2014
18. Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), 2014

Journal Editor / Guest Editor

1. Guest editor of special issue on System-level Synthesis, IEEE Access, 2016

Panelist

1. Panelist for NSF CCF program, 2015, 2017

Conference/Workshop Session Chair

1. Session "Managing Energy in Wearable Devices" at International Symposium on Low Power Electronics and Design (ISLPED), San Francisco, California, August 2016.
2. Session "On-the-Go Storage" at International Conference on Massive Storage Systems and Technology (MSST), Santa Clara, California, May 2016.
3. Research session "Memory that Never Forgets" at Design Automation Conference (DAC), Austin, Texas, June 2016

Reviewer/External Reviewer

1. ACM Transactions on Architecture and Code Optimization (TACO), 2015 - present
2. IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2015 - present
3. Journal of Low Power Electronics and Applications (JLPEA), 2015 - present
4. Elsevier Parallel Computing (PARCO), 2015 - present

5. IEEE Transactions on Computers (TC), 2014 - present
6. IEEE/ACM International Symposium on Microarchitecture (MICR0), 2017
7. IEEE International Symposium on Circuits and Systems (ISCAS), 2016
8. International Symposium on Computer Architecture (ISCA), 2015
9. ACM/IEEE Design Automation Conference (DAC), 2011, 2012, 2015
10. International Conference on Parallel Processing (ICPP), 2015
11. International Conference on Parallel Architectures and Compilation Techniques (PACT), 2013
12. International Symposium on High-performance Computer Architecture (HPCA), 2013
13. Design Automation and Test in Europe (DATE), 2012

University Services

1. Advisory Board at UCSC Silicon Valley campus , 2016

Teaching

Fall 2016	CMPE 110 Computer Architecture (Undergraduate class)
Spring 2016	CMPE 290N Topics in Computer Performance (Graduate class)
Winter 2016	CMPE 110 Computer Architecture (Undergraduate class)
Fall 2015	CMPE 110 Computer Architecture (Undergraduate class)
Spring 2015	CMPE 202 Computer Architecture (Graduate class)

Supervising

Matheus Ogleari	Ph.D.	Fall 2013 -
Xiao Liu	Ph.D.	Fall 2015 -
Mengjie Li	Ph.D.	Fall 2016 -
Hengyu Zhao	Ph.D.	Fall 2016 -
Naga Venkata Sai Indubhaskar Jupudi	Master	Graduated in 2017
Borui Wang	Master	Graduated in 2016
Yiqiao Hu	Master	Graduated in 2016