SiGeC/Si superlattice microcoolers

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Monolithically integrated active cooling is an attractive way for thermal management and
temperature stabilization of microelectronic and optoelectronic devices. SiGeC can be lattice
matched to Si and is a promising material for integrated coolers. SiGeC/Si superlattice structures
were grown on Si substrates by molecular beam epitaxy. Thermal conductivity was measured by the
3ω method. SiGeC/Si superlattice microcoolers with dimensions as small as 40 µm × 40 µm were
fabricated and characterized. Cooling by as much as 2.8 and 6.9 K was measured at 25 °C and
100 °C, respectively, corresponding to maximum spot cooling power densities on the order of 1000
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Thermoelectric (TE) refrigeration in a solid-state active cooling method with high reliability. Bi2Te3-based TE cool-
ers are widely used for cooling and temperature stabilization of microelectronic and optoelectronic devices, but their pro-
cessing is a bulk technology and is incompatible with inte-
grated circuit fabrication process. Solid-state coolers mon-
olithically integrated with microelectronic and optoelectronic devices are an attractive way to achieve compact and effi-
cient cooling. It can lower the cost of fabrication and pack-
aging, and can selectively cool individual key devices in-
stead of the whole chip. However, the thermoelectric figure
of merit (ZT) is quite low for most of the semiconductors
used in microelectronics and optoelectronics. This makes it
difficult to get high cooling performance. Recently hetero-
structure thermionic and superlattice coolers have been pro-
posed, and theoretical calculations show that large improve-
ments in ZT can be achieved and efficient refrigeration
becomes possible with coolers made of conventional semi-
conductor materials.1–8

More recently, a factor of seven enhancement of ZT relative to bulk Si was measured for a Si/Ge superlattice.9
SiGe/Si superlattice coolers have also been demonstrated with a maximum cooling of 7.2 K at 150 °C.10,11 Due to the
larger lattice constant of germanium compared to silicon (4.2%), Ge and SiGe grown on silicon are compressively strained, thus buffer layers are required for thick SiGe and SiGe/Si superlattice layers. This increases the cost of mate-
rial growth and the complexity of integration with Si-based devices. By adding a small amount of carbon into the SiGe material system, strain can be adjusted due to the small lat-
tice constant of carbon. By properly selecting the Ge and C ratio, SiGeC can be lattice matched to silicon, and thick
SiGeC or SiGeC/Si superlattice can be directly grown on Si
without strain. Furthermore, while most of the band offset
between SiGeC and Si lies in the valence band, its conduc-
tivity band offset is larger than that between SiGe and Si.12,13
This makes it possible to use thermionic emission to enhance
the TE cooling for both n- and p-type SiGeC/Si materials.1–4
In this letter, we report the experimental results on SiGeC/Si
superlattice microcoolers. Superlattice structures can im-
prove the cooler performance by reducing the thermal con-
ductivity between the hot and the cold junctions14,15 and by
selective emission of hot carriers above the barrier layers in
the thermionic emission process. Si-based microelectronic
devices can be monolithically integrated with these coolers
to achieve better performance and reliability.

The SiGeC/Si superlattice sample was grown in a Perkin–Elmer Si molecular beam epitaxy (MBE) system ca-
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10 nm in thickness) grown at 500 °C, lattice matched to the Si substrate. The superlattice was doped with Sb to approximately 2 × 10^{19} \text{cm}^{-3}. Finally, the sample was capped with 100 nm Si:Sb, grown at 460 °C and doped to approximately 1 × 10^{20} \text{cm}^{-3}. A cross sectional transmission electron microscopy image of a grown SiGeC/Si superlattice cooler sample is shown in Fig. 1.

The thermal conductivity is a key parameter for thermoelectric materials. The TE device performance increases with a decrease in thermal conductivity. Thin films and nanostructures have been used to reduce the thermal conductivity via acoustical phonon confinement and interface scattering. The 3ω method was used to measure the cross-plane thermal conductivity of the Si_{0.89}Ge_{0.10}C_{0.01}/Si superlattice. The result is 0.085 W/cm K, which is over one order lower than that of Si (1.5 W/cm K).

The processing of SiGeC/Si microcoolers is compatible with an integrated circuit fabrication process. The schematic diagram of the cooler device structure is shown in Fig. 2. Microcoolers were thermally isolated by dry etching mesa structures down to the n⁺ Si substrate. Metallization was made on the mesa and the Si substrate for cathode and anode contacts, respectively. The main part of the cooler structure is the 2 μm thick superlattice. Its low electrical resistance requires low contact resistance for optimum device performance. Ti/Al metallization was used for ohmic contact. This was followed by annealing at 450 °C for 5 s. Specific contact resistivity of 1.5 × 10^{-7} \Omega \text{cm}^2 was measured by transfer length method.

SiGeC/Si superlattice microcoolers with various mesa sizes ranging from 40 × 40 to 100 × 100 μm² were fabricated on one wafer. They were tested on a temperature-controlled heat sink, which was set at a constant temperature during device testing. Device cooling was measured with micro thermocouples on top of the device and was relative to the values at zero current. Figure 3 displays the measured cooling on top of the devices as a function of current with the heat sink at 25 °C. 2.8 K cooling was obtained for the 40 × 40 μm² devices. The test results show that the maximum cooling temperature increases as the device size decreases. This cannot be explained with ideal thermoelectric or thermionic models, and is due to the three-dimensional nature of current and heat spreading in the substrate. The Si substrate of the cooler devices is 500 μm thick and its thermal resistance for the micro devices is about inversely proportional to the square root of the device area. On the other hand, the thermal resistance of the SiGeC/Si superlattice layer is inversely proportional to the device area. This different size dependence makes the effect of the nonideal heat sink smaller for smaller size devices.

For comparison, Si microcoolers were fabricated on n⁺ Si substrates with similar device structure and processing. The results of the 40 × 40 μm² Si devices are shown in Fig. 4 along with those of the SiGeC/Si superlattice coolers of the same size. Over three-fold improvement in maximum cooling is observed for SiGeC/Si superlattice coolers over Si ones.

SiGe is a good TE material for high temperature applications. The SiGeC/Si microcoolers also show better performance at higher temperatures. Figure 5 shows the measured cooling for 50 × 50 μm² SiGeC/Si microcoolers at various heat sink temperatures. The maximum cooling increases from 2.5 K at 25 °C to 6.9 K at 100 °C.

The maximum cooling power density is given by

\[ Q = \kappa (\Delta T_{\text{max}} - \Delta T) / d, \]

where \( \kappa \) and \( d \) are the thermal conductivity and the thickness.
of the superlattice, while $\Delta T_{max}$ and $\Delta T$ are the maximum and actual cooling temperature across the superlattice. At zero $\Delta T$, the coolers have the largest cooling power. Since the majority of the cooling happens over the 2 $\mu$m SiGeC/Si superlattice layer, several degrees of cooling corresponds to maximum cooling power densities on the order of 1000 W/cm² at zero temperature difference.

The maximum cooling temperature of the SiGeC/Si superlattice microcoolers is limited by the contact resistance, Joule heating and heat conduction from the metal wire connected to the cold junction of the cooler, and the low ZT of the Si substrate. These can be solved by increasing the superlattice thickness, making $n$-type and $p$-type cooler arrays and substrate removal, respectively. Fundamentally, the cooler performance is determined by the TE ZT of the cooler materials. A superlattice gives more freedom in material engineering both electrically and thermally, and enables one to enhance the thermoelectric cooling by thermionic emission, 1–4 quantum confinement, 5–8 carrier pocket engineering, 7,8 and phonon engineering. 16,17 The structure and doping of the SiGeC/Si superlattice studied here have not been optimized yet. With optimized material and device design and packaging, cooling up to tens of degrees is possible. Furthermore, SiGeC/Si superlattices can be lattice matched to Si, and SiGeC/Si microcoolers can be monolithically integrated with Si-based devices to achieve compact and efficient localized cooling.

In summary, a lattice matched SiGeC/Si superlattice was grown on Si by MBE and SiGeC/Si superlattice microcoolers were demonstrated. Cooling by as much as 2.8 and 6.9 K was measured at heat sink temperatures of 25 °C and 100 °C, respectively, corresponding to maximum cooling power densities on the order of 1000 W/cm².

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