# Power Trace: An Efficient Method for Extracting the Power Dissipation Profile in an IC Chip From Its Temperature Map

Xi Wang, Sina Farsiu, Peyman Milanfar, *Senior Member, IEEE*, and Ali Shakouri

***Abstract*—In this paper, we present a new technique to calculate the power dissipation profile from the IC temperature map using a process analogous to image processing and restoration. In this technique, finite-element analysis (FEA) is used to find the heat-point spread function (heat PSF) of the IC chip. Then, the temperature map is used as input for an efficient image restoration algorithm which locates the sources of strong power dissipation non-uniformities. Therefore, it optimally solves the inverse heat transfer problem, and estimates the IC power map without extensive lab experiments. Our computationally efficient and robust method, unlike some previous techniques, applies to many experimental scenarios. Simulation results on a typical commercial integrated circuit chip confirm the effectiveness of our proposed method.**

***Index Terms*—Heat point spread function (PSF), image restoration, power dissipation profile, temperature profile, thermal inspection, thermal non-uniformity (hot-spot).**

## NOMENCLATURE:

$g$ Temperature map ($^\circ$C).

$n$ Noise ($^\circ$C).

$\underline{f}$ Power dissipation map ($\mathrm{W/cm^2}$).

$H$ Heat PSF ($^\circ\mathrm{C/W}$).

$I$ Unit (identity) matrix.

$S$ Shifting operator.

$p$ Bilateral filter kernel size.

$\alpha$ Scalar weight.

$\mu$ Steepest descent step size.

$\lambda$ Regularization parameter.

*Superscripts:*

$l$ Pixel number in vertical direction.

$m$ Pixel number in horizontal direction.

*Subscripts:*

$x$ Vertical direction.

$y$ Horizontal direction.

$k$ Iteration index.

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X. Wang and P. Milanfar are with the Department of Electrical Engineering, University of California, Santa Cruz, CA 95064 USA.

S. Farsiu is with the Departments of Ophthalmology and Biomedical Engineering, Duke University, Durham, NC 27708 USA.

A. Shakouri is with the Department of Electrical Engineering, University of California, Santa Cruz, CA 95064 USA (e-mail: ali@soe.ucsc.edu).

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## I. INTRODUCTION

THERMAL issues are some of the key factors limiting the performance and reliability of state-of-the-art electronic and optoelectronic devices and integrated circuits. As switching speed increases and device feature sizes are further miniaturized, localized heating problems are exacerbated [1]. Characterization of the temperature profile in an IC chip is a well-established and powerful technique that allows chip designers and process engineers to identify locations with strong temperature non-uniformity, sometimes called *hot-spots*. These hot-spots could be due to either high activity or fabrication failures [1]–[9]. However, a temperature map by itself often fails to provide sufficient information for IC inspection, because the formation of temperature non-uniformities can be highly complex. Note that, since each hot-spot is often contributed by multiple discrete heat sources, the power dissipation profile has to be obtained and studied in order to achieve effective thermal management.

Typically, chip designers provide the power map to the packaging engineers who calculate the temperature map of the chip taking into account the thermal properties of the die and the package. Since the characteristic length scales of the transistors, various functional units, the die, and the package range from nanometers to centimeters, accurate thermal analysis is done using sophisticated finite-element solvers and multi-grid algorithms. To identify fabrication or device failures, the calculated temperature map of the IC chip is compared to a measured one. For a more quantitative analysis of power dissipation and its spatial extent in the hot-spots, a novel iterative method has recently been proposed where the temperature map is calculated for a series of power maps and the best match is experimentally identified [10]. These methods are accurate and useful when a chip contains a few heat sources with simple geometries. However, in the more complex cases of commercial ICs composed of numerous heat sources, the number of parameters involved becomes prohibitively large, making this problem unsolvable even using the adaptive masking technique [10] to accelerate computation. Recently there have been some attempts to calculate

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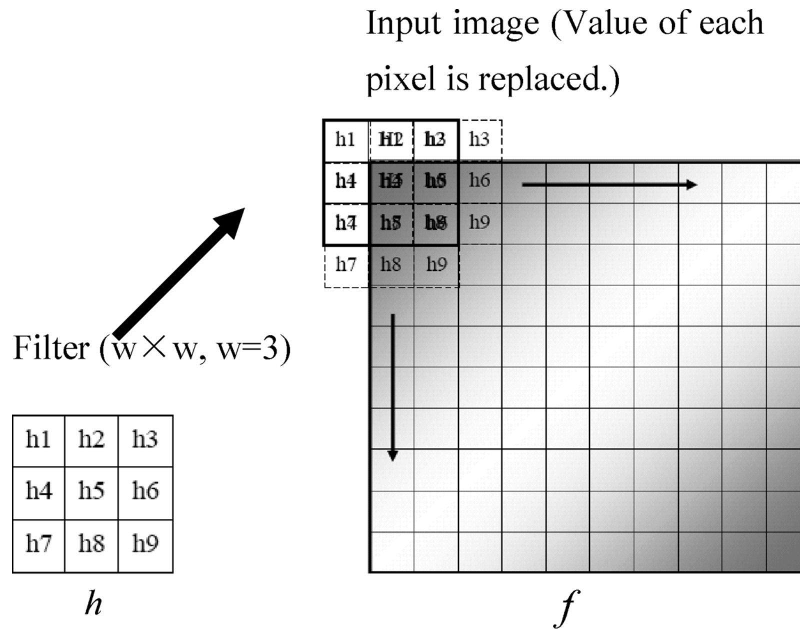


Fig. 1. Concept of spatial filtering.

the power map from the measured temperature map by implementing an experimental direct inverse filter [11]. This is done using extensive characterization of the dies by applying point heat sources at various locations and measuring the resulting temperature maps. However, experimentally obtained point heat source is very sensitive to measurement noise, as well as is limited by spatial resolution of the laser beam. These measurements are inevitably noisy and the problem is numerically *ill-posed*, and the results obtained from such direct inverse filtering technique will always be suboptimal and generally inaccurate [11].

In this paper, by using a process analogous to image processing and restoration, we present a fast numerical solution to this inverse problem, which takes input of the temperature map, and outputs the power map. For a known chip package configuration, the solution is unique. Unlike the method in [10] and[11], our robust technique is much less sensitive to noise and outliers. The organization of this paper is as follows. Section II explains the detailed algorithm of proposed technique. Section III presents a numerical example. Concluding remarks are given in Section IV.

## II. The Optimal Numerical Solution

Extracting the power dissipation profile of an IC chip from its temperature map is done in two steps: first, we estimate the heat point spreading function (PSF) and scaling function, and second, we reconstruct the power map. The details of the proposed algorithm are discussed in the following subsection.

### A. Analogy of Heat Spreading With Image Blurring

The IC chip temperature map is essentially a superposition of the resulting temperature fields of each individual heat source, assuming there are no non-linearities. [12], [13] Therefore, instead of the typical and computationally expensive methods of solving the differential heat conduction equation for the complex structure of a modern IC package, we characterize the heat spreading behavior as a spatial image filtering process. Such spatial filtering technique improves the computation time by a factor of more than a thousand, while accurate within 0 °C [15].

In this approach, the power map is treated as a gray value digital image which is basically a numeric matrix representation of tonal values. As illustrated in Fig. 1, the process of spatial filtering replaces the value of each pixel in the input image (power map) with a new value on the output image (temperature map).

Mathematically speaking, this is a two-dimensional convolution process, which can be described by the following equation:

$$g(x,y) = \sum_{m,l=-a}^{a} h(m,l) f(x+m, y+l) + n(x,y) \qquad (1)$$

where $a = (w-1)/2$ for a $w \times w$ size filter. In the case of simulating heat spreading behavior, the power dissipation profile (power map) on the surface of an IC chip is represented by the matrix $f$. According to (1), by convolving the power map ($f$) with the spatial filter representing the heat point spreading function ($h$), the IC chip temperature map $g$ is estimated. In reality, the temperature measurements are inevitably contaminated by noise ($n$), which we modeled as an additive white Gaussian noise. This is because the main source of noise in a typical thermal image measurement is from the scattered room light, whose spectrum has a Gaussian distribution. However, it will be useful to test the robustness of this technique with other types of noises later on. Therefore, we model $n$ as additive white Gaussian. Note that, when operating around the IC boundaries, a position dependant scaling function effectively scales the heat PSF. This scaling function can be easily estimated by using an FEA tool or a simple analytical approximation as in [15]. This technique has been applied successfully to both static and dynamic temperature profiles [15].

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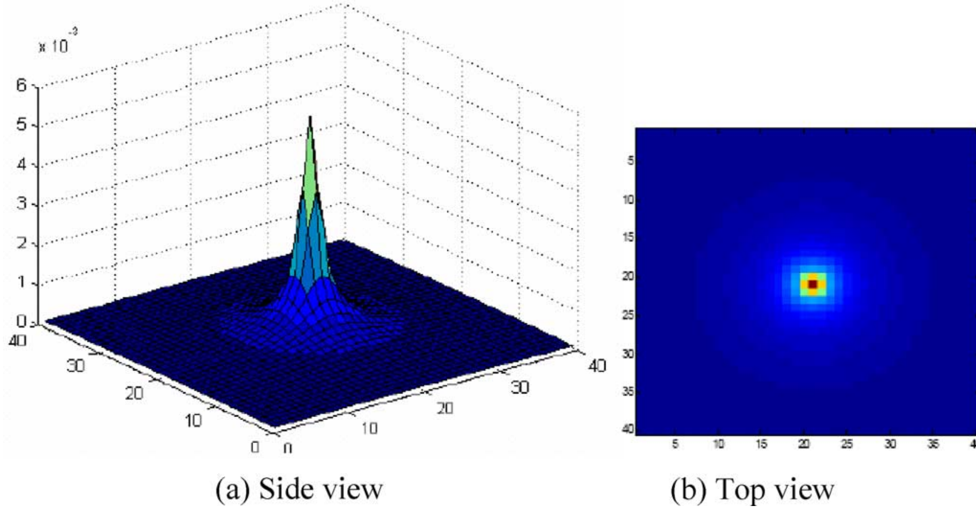


Fig. 2. A 3D illustration of a typical point heat spread function with unit of ($^\circ\mathrm{C/W}$). $\mathrm{X}$ and $\mathrm{Y}$ axis are in units of element (0.025 cm × 0.025 cm/ element).

## B. Heat-Point Spread Function

So far, we have shown that the computationally efficient image spatial filtering technique can be used to accurately calculate the temperature profile in an IC chip. In fact, image blurring is a mathematically rigorous technique as the point spread function used in image analysis is the *Green's function response* of the system. The analytical Green's function can be calculated only when the sample geometry is simple and highly symmetric, while the point-spread function can be calculated numerically and applied to a variety of die sizes and packages. The proposed method in this paper is based on the theory of the Green's function's representative position in a linear system. Therefore, it is generally valid for multiple level inspection, including treating a group of devices as a heat source, as well as treating an individual transistor as a heat source. The question of validation does remain in the regime of heat dissipation within individual transistor. However, that is not in the scope of this paper. In cases where different floorplans of an IC chip are investigated, the heat PSF can be easily parameterized for different configurations [16]. Although multiple heat dissipation paths beside the Si substrate may exist in an IC, the PSF can be found numerically as long as the linearity is preserved on the level of granularity. To find the heat PSF, the temperature spatial impulse response of the system is estimated via the application of a delta function power using an FEA software (ANSYS). A typical heat PSF is shown in Fig. 2.

## C. Power Trace Algorithm

In the previous sections (Sections II-A and II-B), it is shown that the temperature map is related to the power map through a forward model [spatial filtering process of (1)]. Using this forward model, in this section we define an inverse problem to estimate the IC power map from the simulated (or measured) temperature map. The proposed approach for solving this thermal inverse problem, which we call the *Power Trace* algorithm, is inspired from recent image restoration techniques for recovering high quality images from noisy and incomplete measurements [18].

We represent (1) in matrix notation as

$$\underline{g} = \mathbf{H}\underline{f} + \underline{n} \tag{2}$$

where vectors $\underline{g}$ and $\underline{f}$ are the lexicographic representations of the power dissipation profile (power map) and temperature map (simulated or measured) on the surface of an IC, respectively. Matrix $\mathbf{H}$ is the matrix representation of heat PSF kernel ($h$). Finally, the lexicographically ordered vector $\underline{n}$ represents the modeling (or measurement) noise contaminating the temperature map. With this model, the least-squares approach

$$\hat{\underline{f}} = \underset{\underline{f}}{\mathrm{ArgMin}} \left[ \left\| \mathbf{H}\underline{f} - \underline{g} \right\|_2^2 \right] \tag{3}$$

results in a maximum likelihood (ML) estimate, where $\hat{\underline{f}}$ is the reconstructed (estimated) power dissipation map. However, noise and signal are not treated differently in a simple inverse process. This means that even a small amount of noise may result in large perturbations in the final solution [19], which makes the solution unstable.

Therefore, we must consider an efficient regularization term which delivers some general prior information for picking a stable and reliable solution, resulting in the alternative maximum *a posteriori* (MAP) framework [18]. Tikhonov [19] regularization is the most popular regularization term in the image processing literature, which forces spatial smoothness in the estimated image. However, noting that the recovered power map ($\underline{f}$) mimics the shape of the physical heat generating elements with sharp edges, By exploiting non-parametric estimation theory, we are able to show that both Tikhonov and BTV belong to a larger family of regularization terms called Adaptive Kernel (AK) priors [20]. Both Tikhonov and BTV regularization terms are useful priors for the solution of inverse problems such as deblurring. However, using L2 norm-based Tikhonov prior is more appropriate for the cases in which structures present in the unknown image have smooth edges. On the other hand, by incorporating L1 norm in BTV structure,

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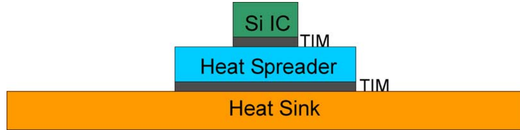


Fig. 3. IC package structure and materials.

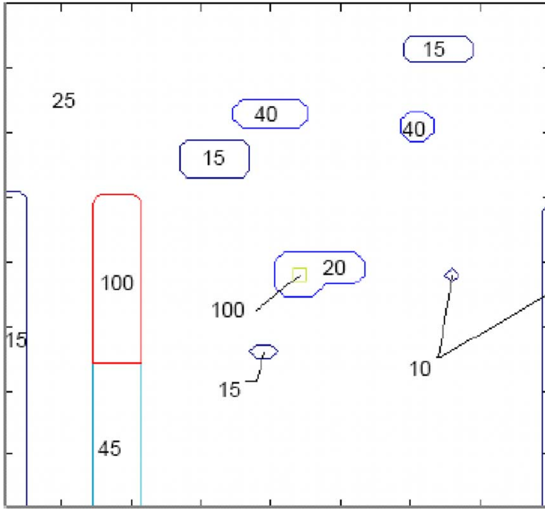


Fig. 4. Power map of the IC chip from design file (1 cm × 1 cm). The regions and numbers in power profile indicate the areas where power is applied (with units of $\mathrm{W/cm^2}$).

the unknown image is assumed to be a collection of piecewise constant tiles. That is to say, the BTV approach is able to accommodate and better reconstruct sharp transitions such as step edges. Such transitions match the present application where the physical heat generating elements have generally sharp edges.

Such an MAP cost function, which outputs the localized power map, is then represented as

$$\underline{\hat{f}} = \underset{\underline{f}}{\mathrm{ArgMin}} \left[ \left\| \mathbf{H}\underline{f} - \underline{g} \right\|_2^2 + \lambda \sum_{m,l=-p}^{p} \alpha^{|m|+|l|} \left\| \underline{f} - S_x^m S_y^l \underline{f} \right\|_1 \right] \tag{4}$$

where the scalar $\lambda$ is the regularization parameter, which properly weights the first term (likelihood cost) against the second term (BTV regularization cost). $S_x^m$ and $S_y^l$ are the operators corresponding to shifting the image represented by $\underline{f}$ by $l$ pixels in the horizontal direction and $m$ pixels in the vertical direction, respectively. The scalar weight $\alpha$ is applied to give a spatially decaying effect to the summation of the regularization terms, as determined by the scalar $p$.

The corresponding steepest descent iterative solution of the minimization problem can be expressed as

$$\underline{\hat{f}}_{k+1} = \underline{\hat{f}}_k - \mu \Bigg\{ \mathbf{H}^T (\mathbf{H}\underline{\hat{f}}_k - \underline{g}) + \lambda \sum_{m,l=-p}^{p} \alpha^{|m|+|l|} [I - S_y^{-l} S_x^{-m}] \mathrm{sign}(\underline{\hat{f}}_k - S_x^m S_y^l \underline{\hat{f}}_k) \Bigg\} \tag{5}$$

where $\mu$ is another scalar defining the steepest descent step size in the direction of the gradient, and $\mathrm{sign}(.)$ is a function representing the element-by-element "sign" operation (replacing the positive elements with 1, the negative elements with $-1$, and zero elements with 0).

TABLE I
MATERIAL THERMAL PROPERTIES (TIM REPRESENTS THERMAL INTERFACE MATERIAL)

| Material | Thermal Conductivity ($W/m-K$) | Thickness ($cm$) |
|---|---|---|
| Silicon | 117.5 | 0.0775 |
| Spreader | 30 | 0.18 |
| Copper | 395 | 0.6 |
| TIM1 | 5.91 | 0.0025 |
| TIM2 | 3.5 | 0.0025 |

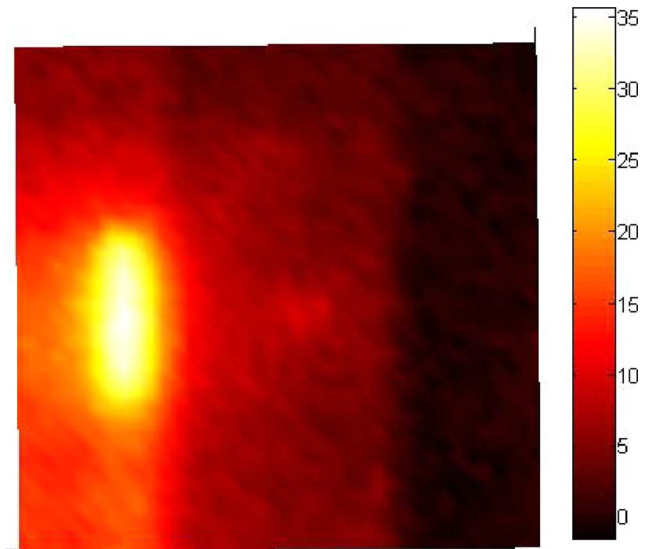


Fig. 5. Temperature map of IC chip (with units of °C).

## III. NUMERICAL RESULTS

By using the algorithm described above we are able to solve the inverse heat spreading problem with high noise tolerance on the input temperature map. We demonstrate the applicability of the proposed technique by testing it on a typical commercial packaged IC chip (Fig. 3). For the purpose of evaluating our results, we obtained the true power map from the designers of the IC chip, which is shown in Fig. 4.

This flip chip package model consists of a 1 cm × 1 cm silicon die IC and a Cu heat sink with an intermittent heat spreading layer surrounded by package lids. The matrix representation of the power map is defined by dividing the die on an orthogonal mesh with congruent elements of size 0.025 cm × 0.025 cm. The material thermal properties and thicknesses of this chip are listed in Table I. Further, the dominant heat transfer path is considered to be through the back of the IC chip and the Cu heat sink. We neglect the heat transfer from the top of the chip through metallization layers and board, assuming it is a relatively small fraction of the total heat dissipation in this simplified example.

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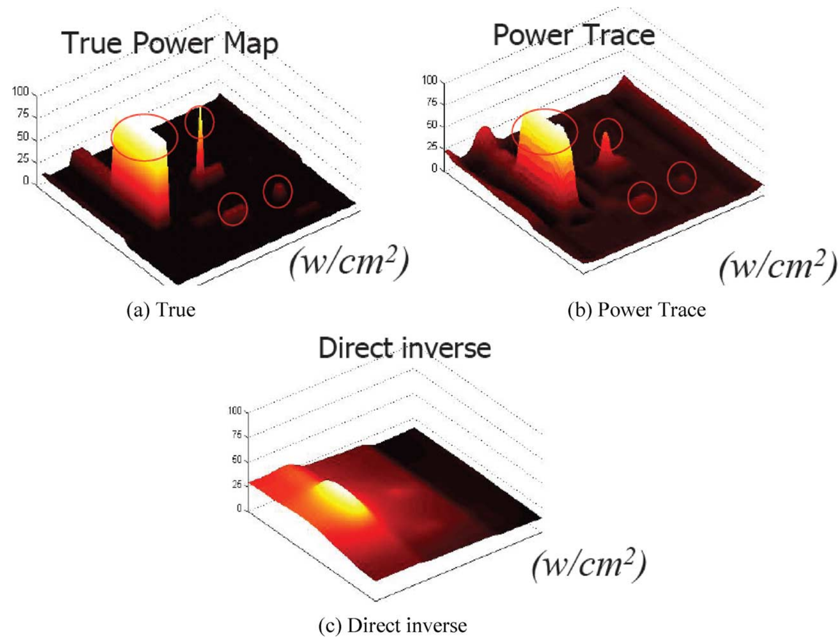


Fig. 6. IC power maps: (a) true (b) extracted using Power Trace algorithm. (c) Extracted using direct inversion.

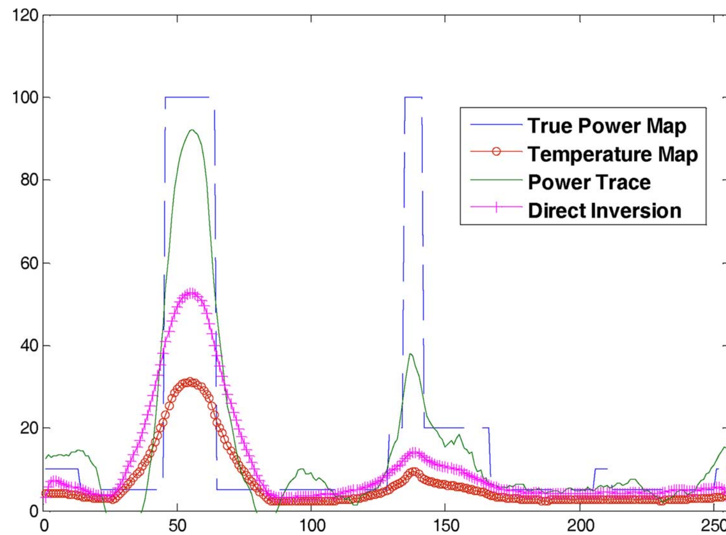


Fig. 7. Cross-section comparison of true power map (dash line), power map extracted using Power Trace (solid line), power map obtained using direct inversion (cross), and the input temperature map (circle) along the center line (horizontal direction).

Following the model in (2), based on the true power map and package structure, we generate a temperature map of the IC chip (Fig. 5).

To define the point heat spread function, we apply a 6.250 $\mathrm{W/cm^2}$ heat flux to a signal element of size $6.25 \times 10^{-4}\ \mathrm{cm}^2$ located at the center of the IC, and calculate the steady-state temperature distribution. The resulting temperature profile is normalized by the amount of heat applied to produce it, with units of $^\circ\mathrm{C/W}$.

The power map of the IC chip is extracted using the proposed Power Trace algorithm that is described in Section II.C, the result of which is shown in Fig. 6(b). Comparing with Fig. 6(a), which is the true power map, the power map extracted by using the Power Trace algorithm remarkably regains the contour of most heating sources and illustrates even the very fine and tiny structures. Such fine details are not resolvable using the direct power map inversion technique of [11], illustrated in Fig. 6(c).

Fig. 7 shows a cross-section comparison of the true power map (dashed line), the power map extracted using the proposed Power Trace method (solid line), the power map obtained using direct inversion method (cross), and the input temperature map (circle) along the center line (horizontal direction). It should be noted that the value at each pixel is represented by a gray value from the image processing perspective.

To demonstrate the applicability of the proposed technique to high power density IC chips and to study the noise tolerance, we modify true power maps from Fig. 4, generate the temperature profile of the same IC chip, and extract power maps using the Power Trace algorithm. Point heat spread function stays the same as in the previous example, since the IC chip structure is identical.

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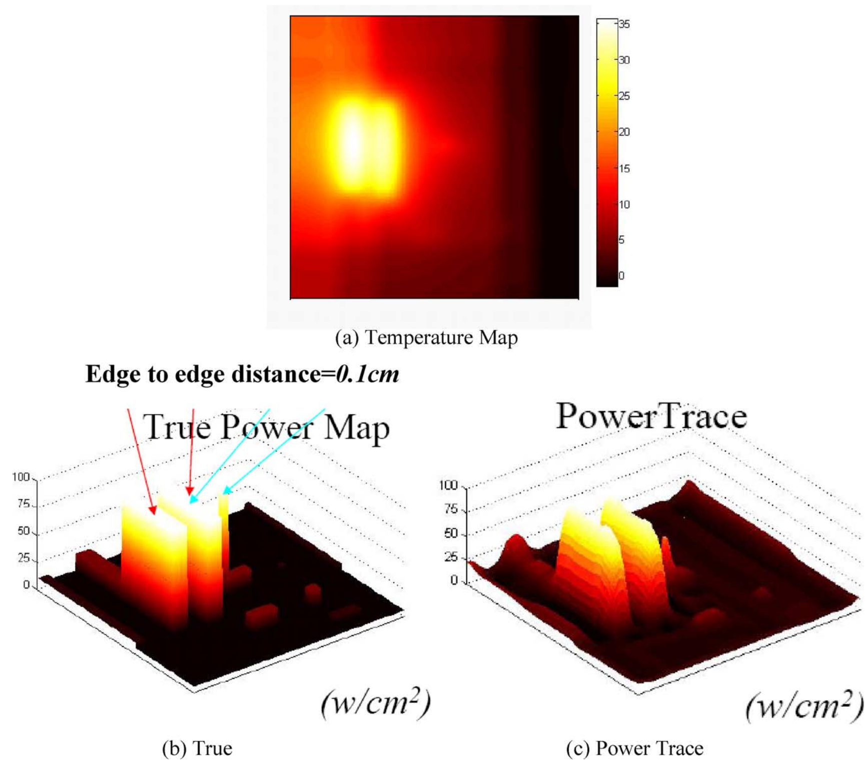


Fig. 8. Applicability of Power Trace algorithm to resolve neighboring heat sources. (a) Temperature map. (b) True power dissipation profile. (c) Extracted power map using Power Trace algorithm.

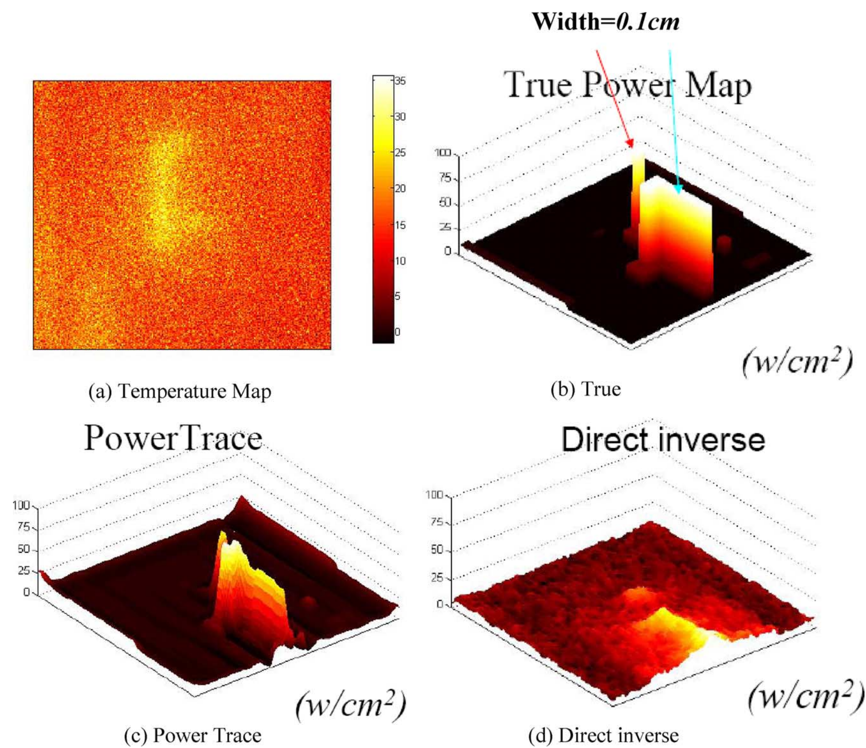


Fig. 9. Noise tolerance of Power Trace algorithm. (a) Temperature map. (b) True power dissipation profile. (c) Extracted power map using Power Trace algorithm. (d) Extracted power map using direct inversion.

The results are shown in Fig. 8. In the modified power map [Fig. 8(b)], three close neighboring power sources, which result in one hot-spot in the temperature map [Fig. 8(a)], are separated from each other by *0.1 cm* in the horizontal direction.

We demonstrate the noise tolerance of Power Trace algorithm in Fig. 9. To simulate heavy noise contamination, zero mean Gaussian white noise with variance of one is added to the generated temperature map, which prohibits a clear vision of the IC

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chip power density distribution. The extracted power map using direct inverse is shown [Fig. 9(c)] as a comparison of the extracted power map using the Power Trace algorithm [Fig. 9(d)].

## IV. CONCLUSION

In this paper, we have presented a new computationally efficient and accurate IC thermal analysis technique for estimating the power dissipation profile from the estimated (or measured) temperature map. This approach was inspired from a recent robust image restoration method [18]. The procedure for applying this new analysis tool requires two simple steps: (1) estimating the heat PSF by using an FEA software or from measurements while using a scaling function to address the boundary effects. This step requires some knowledge about the chip and package dimension and IC's material thermal properties, which are commonly included in the chip/package design files, and (2) exploiting the estimated temperature map and solving an inverse problem to obtain the power map. The inverse problem was solved through an MAP estimation framework in which a robust regularizer is used to stabilize the solution.

Our numerical results have attested to the effectiveness of this technique for identifying the power profile creating temperature non-uniformities. Numerical experiments were preformed on a typical commercial silicon IC package in which the details of power dissipation were unidentifiable using the state-of-the-art technique in the literature [11]. Applicability to identify closely-spaced heat sources in the IC chip and also the tolerance to temperature measurement noise have also been studied in this paper.

The proposed numerical IC thermal analysis technique does not require sophisticated and expensive lab equipments, and is computationally very efficient. Moreover, it is extremely easy to integrate the proposed technique with other electro-thermal analysis algorithms. Furthermore, unlike the methods in earlier literature [10], [11], our technique does not rely on calibration measurements in an actual IC chip. Also, such numerical framework makes it possible to calculate the power maps at much higher resolution compared to the experimentally based techniques. We would also like to note that by coupling the proposed Power Trace technique with in-depth temperature probing methods, such as "Infrared see-through" or "Raman 3–D temperature probing" [1], this 2-D technique can be extended to power mapping in 3-D using volume element (or voxel) matrices.

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**Xi Wang** received the B.S. degree in opto-electronics from Huazhong University of Science and Technology, China, in 2004 and the M.S. degree in electrical engineering from the University of California, Santa Cruz, in 2007, where she is currently working toward the Ph.D. degree.

Her research interests include novel structure transistor thermal management, solid state cooling solution and image processing assisted thermal simulation, and optical thermometry development.

Ms. Wang received the Regent Fellowship from the University of California, Santa Cruz, in 2004 and the Thermal ATW Student Award from the International Microelectronics and Package Society in 2008.

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**Sina Farsiu** received the B.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1999, the M.Sc. degree in biomedical engineering from the University of Tehran, Tehran, in 2001, and the Ph.D. degree in electrical engineering from the University of California, Santa Cruz (UCSC), in 2005.

He was a Postdoctoral Scholar at UCSC from 2006 to 2007 and a Postdoctoral Research Associate in the Department of Ophthalmology, Duke University, Durham, NC, from 2007 to 2009. He is currently an Assistant Professor in the Departments of Ophthalmology and Biomedical Engineering, Duke University. His technical interests include robust image enhancement and reconstruction, computer aided surgery, pediatric ocular imaging and analysis, imaging biomarkers of age-related-macular-degeneration, and optical coherence tomography.

**Peyman Milanfar** (SM'98) received the B.S. degree in electrical engineering/mathematics from the University of California, Berkeley, in 1988, and the S.M., E.E., and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1990, 1992, and 1993, respectively.

Until 1999, he was a Senior Research Engineer at SRI International, Menlo Park, CA. He is currently a Professor of electrical engineering at the University of California, Santa Cruz. He was a Consulting Assistant Professor of computer science at Stanford University, Stanford, CA, from 1998 to 2000, and a visiting Associate Professor there in 2002. His technical interests are in statistical signal and image processing, and inverse problems.

Prof. Milanfar won a National Science Foundation CAREER award in 2000. He is an Associate Editor of the IEEE TRANSACTIONS ON IMAGE PROCESSING and was an Associate Editor for the IEEE SIGNAL PROCESSING LETTERS from 1998 to 2001. He is a member of the Signal Processing Society's Image, Video, and Multidimensional Signal Processing (IVMSP) Technical Committee.

**Ali Shakouri** received the Diplome d'Ingenieur from the Ecole Natoinale Superiere des Telecommunications, Paris, France, in June 1990 and the Ph.D. degree in applied physics and electrical engineering from the California Institute of Technology, Pasadena, in July 1995.

Currently, he is a Professor of electrical engineering at the University of California, Santa Cruz. His current research is on nanoscale heat and current transport in semiconductor devices, high resolution thermal imaging, micro refrigerators on a chip and waste heat recovery. He is also working on a new sustainability curriculum in collaboration with colleagues in engineering and social sciences. He has initiated an international summer school on renewable energy sources in practice. He is the director of the Thermionic Energy Conversion Center, a multiuniversity research initiative aiming to improve direct thermal-to-electric energy conversion technologies. He is the author or coauthor of more than 200 journal and conference papers.

Dr. Shakouri received the Packard Fellowship in Science and Engineering in 1999, the NSF CAREER award in 2000, and the UCSC School of Engineering FIRST Professor Award in 2004.

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