Yuxiong Zhu

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Education Background

- **University of California, Santa Cruz**, California, USA
  PhD, Computer Engineering
- **SUNY at Stony Brook**, New York, USA
  M.S., Electrical Engineering, December 2012
  GPA: 3.93/4.0
- **Tianjin Polytechnic University**, Tianjin, China
  B.S., Electronic and Information Engineering, July 2010
  GPA: 79.27/100

Honors and Awards

- First-class scholarship for excellent students of Tianjin Polytechnic University, 2010
- Third-class scholarship for excellent students of Tianjin Polytechnic University, 2008
- Third-class scholarship for excellent students of Tianjin Polytechnic University, 2007

Research Interests

- My research interests are in Computer Architecture, especially in memory and processors.
- My recent research interests focus on 3D Die-stacked Processing-In-Memory (PIM)

Computer Tools and Skills

- NCverilog, VCS, ISE design suite, ModelSim, Virtuoso, Calibre
- SVN, Visio, Vim Editor, Linux
- Verilog, SystemVerilog, TCL, SystemC, C/C++, Matlab

Work Experience

MediaTek Inc., Beijing, China
Senior IC Verification Engineer Sep. 2014–Jul. 2015
Verification of 3G (WCDMA and TD-SCDMA) wireless baseband data processing modules

- Wrote the test plan according to the design
- Built up the UVM based testbench and the simulation environment
- Co-worked with design, algorithm and DSP firmware teams to accomplish the baseband data chain verification

Inspur Group Co., Ltd., Beijing, China
ASIC Design Engineer Sep. 2013–Sep. 2014
FPGA design of a 6.4GHz Quickpath Interconnect (QPI) Physical layer

- Designed, synthesized, mapped, placed and routed the QPI physical layer using Xilinx ISE

- Implemented main functions including lane deskew, linkwidth configuration and data scramble/descramble
- Verified the functions by running tests on the board which connects two CPUs using two QPI Physical layers

A non-blocking 8 way pipelined Directory Cache

- The cache is used in the node controller which implements the Directory-based Cache Coherence Protocols
- Designed the main parts of the cache
- Proposed the scheme of a non-blocking cache which has the ability to work on other requests while waiting for memory to supply misses
- Implemented special handling of misses with same tags for reducing miss penalties
- Applied LRU policy for replacement
- Designed a hierarchical testbench using SystemVerilog
- Verified the cache based on constrained-random tests

Related Experience

Stony Brook University, Stony Brook, NY

Dual-issue pipelined synergistic processor unit Aug. 2012–Feb. 2013

- Designed the processor unit
- Implemented register forwarding and pipeline stalls to deal with hazards
- Designed 128-bit SIMD Execution Units: Floating Point Adder, Floating Point Multiplier, Funnel Shifter, Fused Multiply-add Unit based on Carry-save Adders, Flagged Prefix Adder for Calculating Absolute Difference

A full custom pipelined synchronous 4-bit carry-select adder Aug. 2012–Dec. 2012

- Designed the schematic and layout using Virtuoso in 0.6um technology
- Verified and measured the functionality and performance using Spectre. The maximum operating clock frequency measured is 1.1GHz
- Designed dynamic DFFs based on TSPC Topology, which are used to achieve shorter Clock-to-Q Delay
- Utilized diffusion sharing and transistors folding to reduce parasitic capacitance

System modeling of a 4 nodes communication system Feb. 2012–May 2012

- Led a project group
- Made plans and allocated tasks
- Designed the main parts and verified the system using SystemC

An 8-bit, 5-MS/s pipelined analog-to-digital converter Feb. 2012–May 2012

- Designed the converter using Virtuoso Schematic Composer in a 0.5-μm CMOS technology
- Designed the schematics of following modules: 90dB Folded-cascode operational amplifiers, a switched capacitor amplifier and comparators with latch
- Analyzed data acquired from simulation using Matlab