

# Current-injection Josephson latch employing a single-flux quantum. I

Jun'ichi Sone and Toshishige Yamada

Microelectronics Research Laboratories, NEC Corporation, Miyazaki, 4-1-1, Miyamae-ku, Kawasaki, Kanagawa 213, Japan

(Received 5 November 1985; accepted for publication 17 January 1986)

A new current-injection Josephson latch employing a single-flux quantum is proposed. It has a master-slave circuit configuration and operates under ac power supply. In the circuit, data are stored as a circulating current in a superconducting loop consisting of a single junction and inductances. A two-junction interferometer gate directly coupled to the loop reads out the stored data. Dual-rail signals are generated from the read-out data by Josephson junctions and resistor-coupled Josephson logic gates. The isolation between a master circuit and a slave circuit is realized using high-impedance states in the Josephson junctions. The circuit design and computer-simulation results on the circuit operation are described in this paper.

## I. INTRODUCTION

Josephson devices are attractive circuit elements for ultrahigh performance computer applications. Their high performance is based on the high intrinsic switching speeds, low-power dissipation, and impedance-matched superconducting transmission lines inherent to the Josephson technology. These features have been demonstrated by various types of Josephson logic circuits.<sup>1-7</sup> Among them, current injection Josephson logic gates<sup>3-7</sup> have various advantages over magnetically coupled Josephson logic gates,<sup>1,2</sup> with regards to small device sizes, intrinsically damped resonance phenomena, and reduced fan-out delay time. These Josephson logic gates operate most commonly in a latching mode. In order to reset these latching logic gates to the "off" state (superconducting state), lowering their supply currents to zero is required. Thus, Josephson latch circuits, which store data during the time interval when the supply currents are turned off, are required to implement the Josephson logic circuits.

Several kinds of the latch circuits have been reported.<sup>8,9</sup> Most of them use the magnetically coupled interferometer circuits. Because of the magnetically coupled transformer used, these circuits may occupy relatively large areas on a chip. The Josephson logic circuits constructed from the magnetically coupled latches and the current injection logic gates make the circuit design and fabrication complicated, and the advantages of the current injection logic gates described above cannot be fully taken. From the points of the smallness in the device size and the compatibility in the circuit design and fabrication processes, current injection Josephson latches are desirable to be realized for fully current injection logic circuits.

Recently, we have originated a current injection Josephson latch circuit employing a single-flux quantum, and successfully verified its proper operation in a experimentally fabricated latch circuit. Its main features are the capability of high-speed operation and the smallness of the device size. In this paper, we present the operation principle and circuit design of the novel current injection Josephson latch circuit. In the circuit, data are stored as a circulating current in a loop consisting of a single junction and inductances. A two-junction interferometer gate is directly coupled to the loop

and reads out the stored data. The dual-rail signals are generated from the read-out data by Josephson junctions and the resistor-coupled Josephson logic (RCJL) gates.<sup>7</sup> The circuit design, as well as operation principle, are described in Sec. II. Its proper operation is investigated using computer simulations in Sec. III. Conclusions are given finally in Sec. IV. Experimental verifications of this latch circuit including its high-speed operation will be presented in a companion paper.<sup>10</sup>

## II. LATCH CIRCUIT OPERATION

The basic circuit configuration of the current injection latch is shown in Fig. 1. It has a master-slave configuration and is designed to operate under a trapezoidal ac power supply shown in Fig. 2.<sup>11</sup> The function of the present latch circuit is the same as those of the magnetically coupled latch circuits previously reported.<sup>9</sup> The flat portion of the power supply waveform, called the active portion of the machine cycle, is the nominal operating region for the logic gates. The outputs of these logic gates are stored in the master circuit, before the power supply begins its transition into the opposite polarity. The master circuit holds the data during the time interval when the ac power supply changes its polarity.

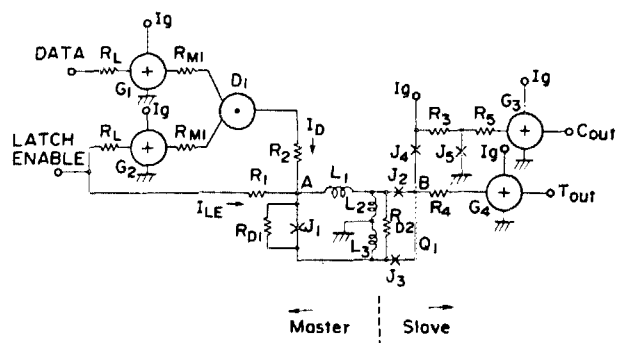


FIG. 1. Equivalent circuit of a latch circuit.  $G_1, G_2, G_3, G_4$ —OR gates.  $D_1$ —AND gate. DATA—Data signal. LATCH ENABLE—Latch enable signal.  $I_1 = 0.3$  mA,  $I_2 = I_3 = 0.15$  mA,  $I_4 = I_5 = 0.21$  mA,  $L_1 = 5.3$  pH,  $L_2 = 2.3$  pH,  $R_{D1} = 1.0$   $\Omega$ ,  $R_{D2} = 1.0$   $\Omega$ ,  $R_3 = R_4 = 6.0$   $\Omega$ ,  $R_5 = 2.0$   $\Omega$ ,  $R_L = 6.0$   $\Omega$ ,  $R_M = 4.0$   $\Omega$ ,  $R_1 = R_2 = 5.0$   $\Omega$ .

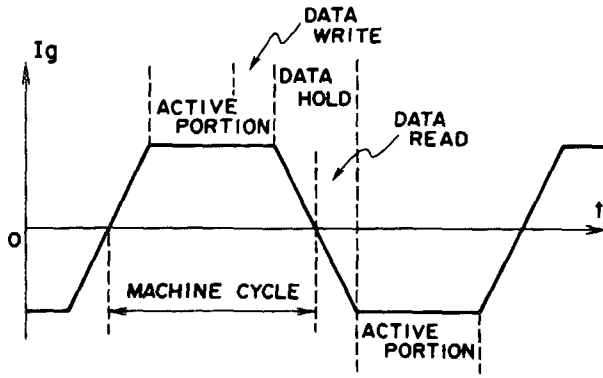


FIG. 2. The operation of a latch circuit under ac power supply.

A slave circuit detects the data stored in the master circuit during the power supply ramp of the next cycle, and holds the data at its output until the end of the cycle, allowing the latch to accept new data during the cycle.<sup>9</sup>

### A. Master circuit

The master circuit consists of two RCJL OR gates  $G_1$  and  $G_2$ , a RCJL AND gate  $D_1$ , a superconducting loop, and a sense gate  $Q_1$ . The loop is composed of a single-junction  $J_1$  and inductances  $L_1$ ,  $L_2$ , and  $L_3$ . A damping resistor  $R_D$  is connected parallel to the junction  $J_1$ . The interferometer sense gate  $Q_1$  consists of the inductances  $L_2$  and  $L_3$ , junctions  $J_2$  and  $J_3$ , and a damping resistor  $R_D$ , and is directly connected to the loop through  $L_2$  and  $L_3$ . The write operation of the master circuit is as follows. A latch enable signal (LE) is injected into the loop and the gate  $G_2$  in the active region of the cycle. Then  $G_2$  switches from the superconducting state ("off") to the voltage state ("on") and an output current is delivered to the AND gate  $D_1$ . The gate  $G_1$  switches to the voltage state upon the application of a data signal (DATA) and delivers an output current to the gate  $D_1$ . Thus only when DATA = LE = 1, the gate  $D_1$  switches and a data output current  $I_D$  is injected into the loop, causing magnetic flux to enter the loop. Then the data is written as a circulating current in the loop.

Here let us investigate the variation of the quantum phase difference  $\theta_1$  of the Josephson junction  $J_1$  in the loop against the external current  $I_e$  injected at the node A in Fig. 1. As explained later in the slave-circuit operation, current injection into the loop from the slave circuit is prohibited in the write operation. It is because either a junction  $J_4$  in the slave circuit or junctions  $J_2$  and  $J_3$  in the sense gate  $Q_1$  switch into the voltage state and present a high resistance. When the junction  $J_4$  is in the high-resistance state, the flux quantization condition and the current continuation condition give the equations for  $I_e$  and the quantum phase differences  $\theta_1$ ,  $\theta_2$ , and  $\theta_3$  of the junctions  $J_1$ ,  $J_2$ , and  $J_3$  as

$$(\phi_0/2\pi)(\theta_1 + \theta_3 - \theta_2 + 2n\pi) = (I_e - I_1 \sin \theta_1)L_1, \quad (1)$$

$$(\phi_0/2\pi)(\theta_2 - \theta_3 + 2m\pi) = (I_e - I_1 \sin \theta_1 - I_2 \sin \theta_2)L_2 - (I_1 \sin \theta_1 - I_3 \sin \theta_3)L_3, \quad (2)$$

$$I_2 \sin \theta_2 = I_3 \sin \theta_3, \quad (3)$$

where  $I_1$ ,  $I_2$ , and  $I_3$  are the Josephson critical currents of the junctions  $J_1$ ,  $J_2$ , and  $J_3$ , respectively,  $\phi_0$  is the magnetic-flux quantum,  $L_1$ ,  $L_2$ , and  $L_3$  are the inductances shown in Fig. 1, and  $n$  and  $m$  are integers for restricting the phases to the range  $-\pi < \theta_i < \pi$ . The stability condition due to a minimum of potential energy is obtained as<sup>12</sup>

$$\begin{aligned} & \cos \theta_1 \cos \theta_2 \cos \theta_3 + \frac{\phi_0}{2\pi} \cos \theta_1 \left( \frac{\cos \theta_2}{I_3} + \frac{\cos \theta_3}{I_2} \right) \\ & \times \left( \frac{1}{L_1} + \frac{1}{L_2 + L_3} \right) + \frac{\phi_0}{2\pi} \frac{1}{L_1 I_1} \cos \theta_2 \cos \theta_3 \\ & + \left( \frac{\phi_0}{2\pi} \right)^2 \frac{1}{L_1 I_1} \left( \frac{1}{L_2 + L_3} \right) \left( \frac{\cos \theta_2}{I_3} + \frac{\cos \theta_3}{I_2} \right) > 0. \quad (4) \end{aligned}$$

In the derivation of the above equations, we have neglected the subgap current flowing in the junction  $J_4$ . Here, we assume  $I_2 = I_3$  and  $L_2 = L_3$ , therefore, the sense gate  $Q_1$  has a symmetric threshold characteristics. From the Eqs. (1)–(3), we can obtain

$$\theta_2 + \theta_3 = 2k\pi, \quad (5)$$

$$(I_e/I_1) - \sin \theta_1 = \lambda_1(\theta_1 - 2\theta_2 + 2n'\pi), \quad (6)$$

$$(I_e/I_1) - 2 \sin \theta_1 - 2(I_2/I_1) \sin \theta_2 = \lambda_2(2\theta_2 + 2m'\pi), \quad (7)$$

$$\lambda_1 = \phi_0/2\pi L_1 I_1, \quad (8)$$

$$\lambda_2 = \phi_0/2\pi L_2 I_1, \quad (9)$$

where  $k$ ,  $n'$ , and  $m'$  are integers. Introducing  $\phi_1 = \theta_1 + 2n'\pi$ , Eqs. (5)–(7) can be rewritten as

$$I_e/I_1 = \sin \phi_1 + \lambda_1 \phi_1 - 2\lambda_1 \theta_2, \quad (10)$$

$$I_e/I_1 = 2\lambda_2 \theta_2 + 2(I_2/I_1) \sin \theta_2 + 2 \sin \phi_1 + 2\lambda_2 m'\pi. \quad (11)$$

Then,

$$\begin{aligned} & 2(\lambda_1 + \lambda_2)\theta_2 + 2(I_2/I_1) \sin \theta_2 \\ & = \lambda_1 \phi_1 - \sin \phi_1 - 2\lambda_2 m'\pi. \quad (12) \end{aligned}$$

Since Eq. (12) gives  $\theta_2$  as a function of  $\phi_1$ , the relationship of  $\phi_1$  against  $I_e$  can be numerically calculated. In Fig. 3 are shown the calculated  $I_e - \phi_1$  characteristics with typical circuit parameters depicted in the caption of Fig. 1. Solid lines show the thermodynamically stable operating regions, while broken lines show the unstable ones. There were no solutions of  $\theta_2$  in Eq. (12) except with  $m' = 0 \pm 1$ .

In the absence of the external current  $I_e$ , five stable operating points, such as A, B, C, all with  $m' = 0$ , D with  $m' = 1$ , and E with  $m' = -1$  are present. Therefore, a setup operation, described as follows, is required to restrict the  $m'$  value of the operating point to zero. There are no operating points with  $m' = 1$  and  $m' = -1$  for  $I_e < -i_0$  and  $I_e > i_0$ , respectively, where  $i_0$  and  $-i_0$  are the external currents for the operating point F and G in Fig. 3. Thus, once the bipolar external current  $I_e$  with the amplitude larger than  $i_0$  is applied, the operating point only with  $m' = 0$  is allowed to be present. Here, the damping resistance  $R_D$  has been assumed to be sufficiently low so that direct transitions of the operating point between  $m' = 1$  and  $m' = -1$  have not been allowed. When the external current increases from zero, the operating point B moves without changing its  $m'$  value until  $\theta_2 (= -\theta_3)$  reaches  $\pi/2$  from zero. Similarly, the operat-

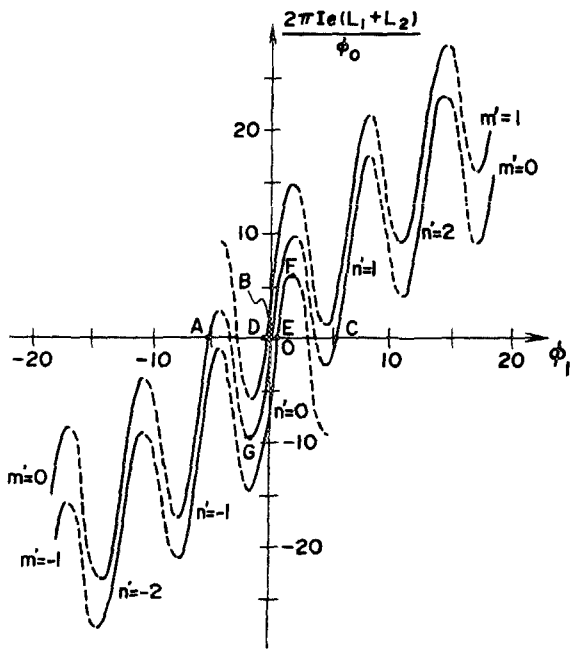


FIG. 3. External current  $I_e$  vs a quantum phase difference  $\phi_1$  of a junction  $J_1$  with a junction  $J_4$  in the resistive state. Solid lines show thermodynamically stable operating region. Broken lines show thermodynamically unstable operating region.

ing point  $B$  moves without changing its  $m'$  value until  $\theta_2$  reaches  $-\pi/2$  from zero, as the external current decreases from zero. In the storage loop with the typical parameters shown in Fig. 1, the operating point with  $m' = 0$  moves among modes with  $n' = 0, \pm 1, \pm 2$  without changing its  $m'$  value when the external current varies.

When the junctions  $J_2$  and  $J_3$  are in the resistive state, the flux quantization condition and the stability condition are

$$\begin{aligned} I_e(L_1 + L_2) - I_1(L_1 + 2L_2) \sin \theta_1 \\ = (\phi_0/2\pi)(\theta_1 + 2n''\pi) \\ \equiv (\phi_0/2\pi)\phi_1, \end{aligned} \quad (13)$$

$$I_1(L_1 + 2L_2) \cos \theta_1 + (\phi_0/2\pi) \geq 0, \quad (14)$$

where  $n''$  is an integer. Here, we have also neglected the subgap currents flowing in the junctions  $J_2$  and  $J_3$ . The relationship of  $I_e$  and  $\phi_1$  with junctions  $J_2$  and  $J_3$  in the resistive state are also numerically calculated with the same circuit parameters and are shown in Fig. 4 by a solid curve. For reference,  $I_e - \phi_1$  characteristics for  $m' = 0$  with the junction  $J_4$  in the resistive state are also shown by a broken curve. It can be seen that the differences between those curves are small, thus the operation described in the next paragraph can be applied to these two cases.

In the absence of the current injected into the loop, H, I, and J in Fig. 4 are stable operating points. As is evident in the following explanation, the operating point stays at either H or I when the power supply current, including the external current  $I_e$ , had negative polarity in the last machine cycle. In order to reset the storage loop, the latch enable signal is applied in the next cycle with positive polarity, and the operat-

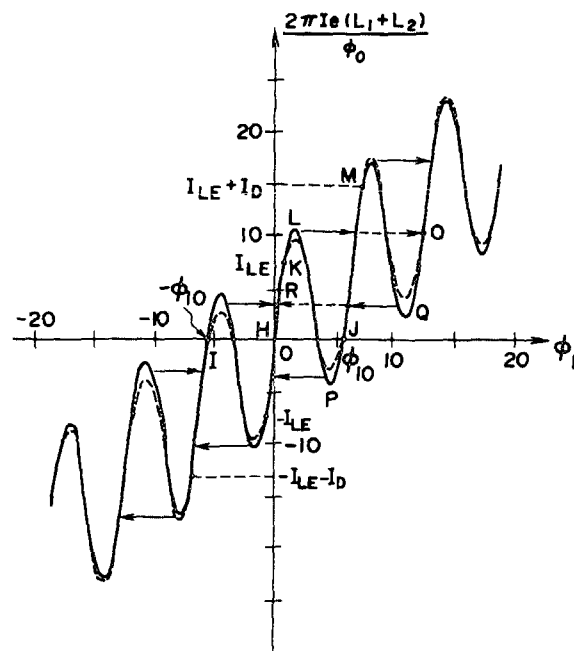


FIG. 4. External current  $I_e$  and a quantum phase difference  $\phi_1$  of a junction  $J_1$ . A solid line represents the operating region when junctions  $J_2$  and  $J_3$  are in the resistive state.

ing point moves from H or I to K. When the data signal is applied, the operating point moves from K to M through L, and the magnetic flux is caused to enter the loop. On the other hand, in the absence of the data signal, the operating point stays at K. At the end of the cycle, all the signals are turned off. Then, the operating point moves to J for DATA "1," while it moves to H for DATA "0." Similar operations are repeated in the following cycle with negative polarity. Thus DATA "1" is represented by the state at I or J, depending upon the power supply polarity. DATA "0" is represented by the state at H. From the values of  $\phi_1$  at I and J, the amplitude of the circulating current  $I_{\text{cir}}$  can be estimated as

$$I_{\text{cir}} = I_0 \sin \phi_{10} \approx 0.7I_0. \quad (15)$$

Since the data output current  $I_D$  and the latch enable current  $I_{LE}$  are additively injected into the loop, the proper write operation of this latch is not affected by the sequence of the activation in the data signal and the latch enable signal.

## B. Slave circuit

The slave circuit consists of junctions  $J_4$  and  $J_5$  with critical currents  $I_4$  and  $I_5$ , the sense gate  $Q_1$ , and RCJL OR gates  $G_3$  and  $G_4$ . Resistors  $R_3$  and  $R_4$  are designed to have the same resistance. The critical currents  $I_4$  and  $I_5$  are chosen to satisfy the relationships of

$$I_g^0/2 < I_4 = I_5 < I_g^0, \quad (16)$$

$$I_m(I_{\text{cir}}) < I_4 = I_5 < I_m(0), \quad (17)$$

where  $I_g^0$  is the absolute value of the gate current in the flat portion of the power supply,  $I_m(0)$  and  $I_m(I_{\text{cir}})$  are threshold gate currents of the gate  $Q_1$  in the absence and presence of the circulating current  $I_{\text{cir}}$  in the loop, respectively.

When DATA "1" is stored in the form of a circulating

current,  $Q_1$  switches before  $J_4$  during the power supply ramp and an output current is injected into the gate  $G_4$  and the junction  $J_5$ . Then  $G_4$  switches, providing "1" at the true output. On the other hand,  $J_4$  and  $J_5$  remain in the superconducting state, since the maximum currents  $I_g^0/2$  flowing in the junctions  $J_4$  and  $J_5$  are less than their critical currents. Thus the output on the complement branch is "0." Since the gates operate in a latching mode, these output states remain unchanged even if the circulating current changes its value during the same cycle. When DATA "0" is stored in the loop,  $J_4$  switches before the gate  $Q_1$  and the supply current to  $Q_1$  is diverted to the junction  $J_5$ . Then  $J_5$  and  $G_3$  switches to the voltage state in this sequence, providing "1" at the complement output. The gate  $Q_1$  does not switch even if the data signal is later entered in the latch during the same cycle, since  $Q_1$  has no supply current after  $J_4$  switching.

Here let us investigate the threshold characteristics of the gate  $Q_1$ . The relationships of the quantum phase differences  $\theta_1, \theta_2$ , and  $\theta_3$  of the junctions  $J_1, J_2$ , and  $J_3$  and the gate current  $I_g$  supplied from node B in Fig. 1 are described as

$$I_1 \sin \theta_1 + (\phi_0/2\pi L_1)(\theta_1 + \theta_3 - \theta_2 + 2n\pi) = 0, \quad (18)$$

$$I_2 \sin \theta_2 + \frac{\phi_0}{2\pi L_1}(\theta_2 - \theta_1 - \theta_3 - 2n\pi) + \frac{\phi_0}{4\pi L_2}(\theta_2 - \theta_3 + 2m\pi) + \frac{I_g}{2} = 0, \quad (19)$$

$$I_2 \sin \theta_3 + \frac{\phi_0}{2\pi L_1}(\theta_1 + \theta_3 - \theta_2 + 2n\pi) + \frac{\phi_0}{4\pi L_2}(\theta_3 - \theta_2 - 2m\pi) + \frac{I_g}{2} = 0, \quad (20)$$

$$\begin{aligned} & \cos \theta_1 \cos \theta_2 \cos \theta_3 + \frac{\phi_0}{2\pi} \cos \theta_1 (\cos \theta_2 + \cos \theta_3) \\ & \times \left( \frac{1}{I_2 L_1} + \frac{1}{2I_2 L_2} \right) + \frac{\phi_0}{2\pi} \frac{1}{I_1 L_1} \cos \theta_2 \cos \theta_3 \\ & + \left( \frac{\phi_0}{2\pi} \right)^2 \frac{1}{2I_1 I_2 L_1 L_2} (\cos \theta_2 + \cos \theta_3) \geq 0. \end{aligned} \quad (21)$$

The condition (21) assures that the solution of Eqs. (18)–(20) is thermodynamically stable. Here let us notice that no external currents are injected from the node A in Fig. 1 during the read operation. Introducing new variables  $\phi_1 = \theta_1 + 2n\pi$ ,  $x = \theta_2 + \theta_3$ , and  $y = \theta_2 - \theta_3$ , we can rewrite Eqs. (18)–(20) as

$$\sin \phi_1 + (1/\nu_1)(\phi_1 - y) = 0, \quad (22)$$

$$2 \sin \frac{x}{2} \cos \frac{y}{2} + \frac{I_g}{I_2} = 0, \quad (23)$$

$$2 \cos \frac{x}{2} \sin \frac{y}{2} + \frac{2}{\nu_2}(y - \phi_1) + \frac{1}{\nu_3}(y + 2m\pi) = 0, \quad (24)$$

where

$$\nu_1 = \frac{2\pi I_1 L_1}{\phi_0}, \quad \nu_2 = \frac{2\pi I_2 L_1}{\phi_0}, \quad \nu_3 = \frac{2\pi I_2 L_2}{\phi_0}.$$

The solution for  $n = m = 0$  is evident, i.e.,

$$\theta_1 = y = 0, \quad (25)$$

$$2 \sin (x/2) + (I_g/I_2) = 0. \quad (26)$$

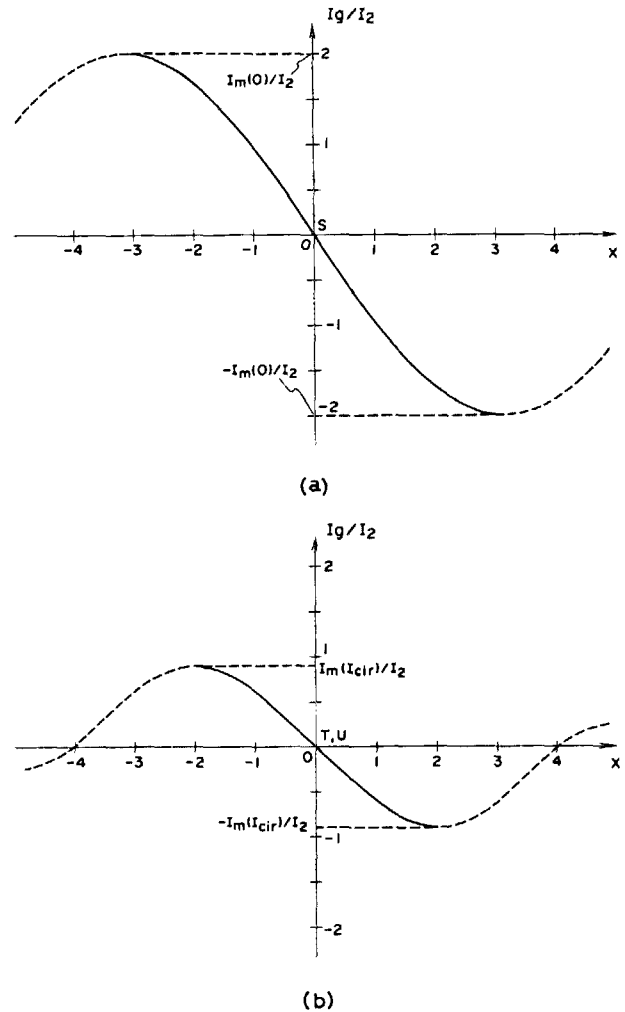


FIG. 5. Gate current for a sense gate  $Q_1$  vs the sum of the quantum phase differences of junctions  $J_2$  and  $J_3$ ,  $x = \theta_2 + \theta_3$ . (a) A curve shows the operating region in the absence of a circulating current in the storage loop. (b) A curve shows the operating region in the presence of a circulating current in the loop. Solid lines in (a) and (b) represent the thermodynamically stable operating region, while broken lines represent the thermodynamically unstable operating region.

In Fig. 5(a), the gate current  $I_g$  is plotted versus  $x$  by a solid line. The broken line shows the thermodynamically unstable solutions. The operating point S in Fig. 5(a) where  $\theta_1 = \theta_2 = \theta_3 = 0$  corresponds to the point B in Fig. 3 where no circulating current is present. Therefore the sense gate  $Q_1$  remains in the superconducting state up to  $|I_g| = 2I_2 [ = I_m(0) ]$  when the absolute value of the gate current increases.

The solutions for  $n = 1, m = 0, n = -1$ , and  $m = 0$  are numerically calculated and the threshold gate current is plotted versus  $x$  in Fig. 5(b) by a solid line. The operating point T with  $\phi_1 = 5.4, \theta_2 = 0.83, \theta_3 = -0.83$  and U with  $\phi_1 = -5.4, \theta_2 = -0.83, \theta_3 = 0.83$  correspond to the points A and C in Fig. 3, respectively, where the nominal circulating current is present. Therefore, the gate  $Q_1$  switches to the voltage state when the absolute value of the gate current exceeds  $I_c [ = I_m(I_{cir}) ]$  in Fig. 5(b).

### C. Circuit design

The circuit parameters of the latch were chosen such as to make the latch compatible with the 5- $\mu\text{m}$  resistor-coupled Josephson logic described earlier.<sup>13</sup> The circuit elements which constitute the storage loop are designed as follows.

(a) In the absence of the current injected into the storage loop, there should be three stable operating points like H, I, and J in Fig. 4. In the optimum design, the absolute values of the external currents for the operating points P and Q in Fig. 4 should be the same. As a result,

$$(L_1 + 2L_2)I_1 \approx \frac{2}{3}\phi_0. \quad (27)$$

(b) The discrepancies between the solid curve and the broken curve in Fig. 4 should be small in order to obtain a wide operating margin for the latch enable current  $I_{LE}$  and the data current  $I_D$ .

(c) The solution for  $\theta_2$  in Eq. (12) with  $-\pi/2 < \theta_2 < \pi/2$  and  $m' = 0$  should be present over the wide range of  $\phi_1$ . This assures that the external current injected into the storage loop can be varied in a wide range with the  $m'$  value kept to zero, resulting in a wide operating margin for the data current. To satisfy the above two requirements (b) and (c), smaller values of  $L_2/L_1$  and  $I_2/I_1$  are desirable.

(d) To maximize the operating margin for the circulating current  $I_{cir}$  in the loop,

$$2L_2I_{cir} \approx 1.4L_2I_1 \approx \phi_0/2. \quad (28)$$

The four conditions of (a)–(d) are not always compatible, i.e., if we follow the requirements (27) and (28), the  $L_2/L_1$  value is determined as  $\sim 3/2$ , which is not necessarily small to satisfy the requirements (b) and (c). The  $I_2/I_1$  value also cannot be reduced unlimitedly, since the output current of the sense gate  $Q_1$  has to drive the OR gate  $G_4$ , and the output current of the AND gate  $D_1$  has to cause the flux quantum to enter the loop. In the present design, the critical current ratio of  $I_2/I_1 = 1/2$  was chosen. The value of  $L_2/L_1$  was chosen such that when the external current  $I_e$  is varied, the operating point can move among the modes of  $n' = 0, \pm 1, \pm 2$  in Fig. 3 with the  $m'$  value kept to zero, i.e., without the absolute value of  $\theta_2$  and  $\theta_3$  exceeding  $\pi/2$ , even if  $\pm 5\%$  deviations of inductances  $L_1, L_2$  and  $\pm 10\%$  deviations of critical current  $I_1$  and  $I_2$  are present.

The circuit parameters for a 5- $\mu\text{m}$  lead-alloy<sup>14</sup> Josephson latch circuit with a Josephson critical current density of 800 A/cm<sup>2</sup> were optimized to obtain wide operating current

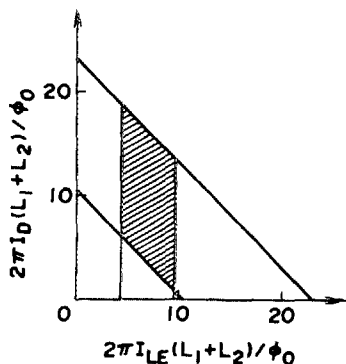


FIG. 6. Operating margins for a latch enable current  $I_{LE}$  and a data current  $I_D$ . Shaded area shows the current region for the proper latch operation.

margins, following the conditions described above. The typical results are shown in the caption of Fig. 1. The optimum damping resistances of  $R_{D_1}$  and  $R_{D_2}$  depend on the dynamics of the storage loop, and were determined by computer simulations, the detail of which is described in Sec. III. As is known in Figs. 3, 4, and 5, the designed operating current margins for the data current  $I_D$ , the latch enable current  $I_{LE}$ , and the supply current  $I_g$  for the junction  $J_3$  and the sense gate  $Q_1$  are comparable to the previously reported magnetic coupled Josephson latches.<sup>9</sup> The current margins for  $I_D$  and  $I_{LE}$  are shown in Fig. 6. The shaded region represents the proper operating region. The designed values and margins for the operating currents are listed as

$$I_D = 0.43 \text{ mA} \pm 39\%, \quad (29)$$

$$I_{LE} = 0.3 \text{ mA} \pm 38\%, \quad (30)$$

$$I_g = 0.3 \text{ mA} \pm 33\%, \quad (31)$$

$$I_m(I_{cir})/I_m(0) = 0.44. \quad (32)$$

### III. COMPUTER SIMULATIONS

The amount of the magnetic flux generated in the loop deeply depends on the damping resistance  $R_{D_1}$ . Appropriate damping resistance  $R_{D_1}$  for the proper operation was determined by computer simulations. In Fig. 7 is shown the simu-

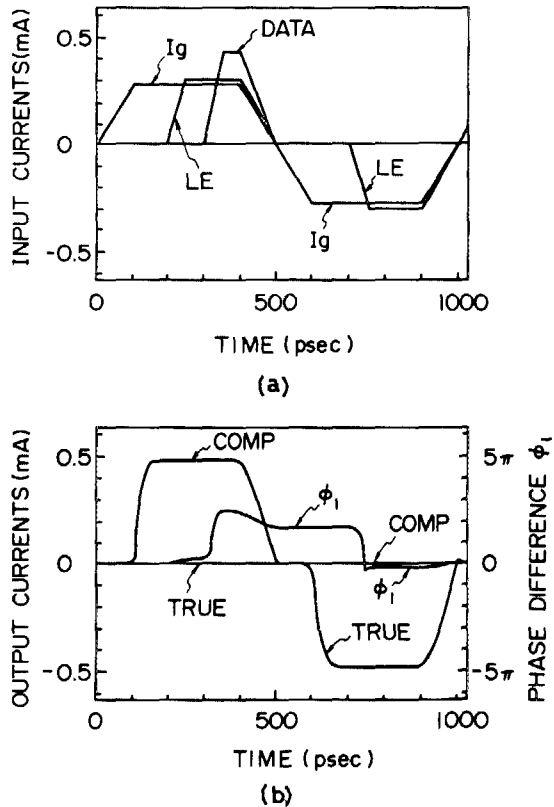


FIG. 7. A two cycle computer simulation of the latch with a damping resistance of 1.0  $\Omega$ . The simulation begins with a zero stored in the latch. (a)  $I_g$ —Gate current for the junction  $J_4$  and the sense gate  $Q_1$ . DATA—Data current. LE—Latch enable current. (b) TRUE, COMP—True and complement output currents of the slave circuit.  $\phi_1$ —Quantum phase difference of the junction  $J_1$ .

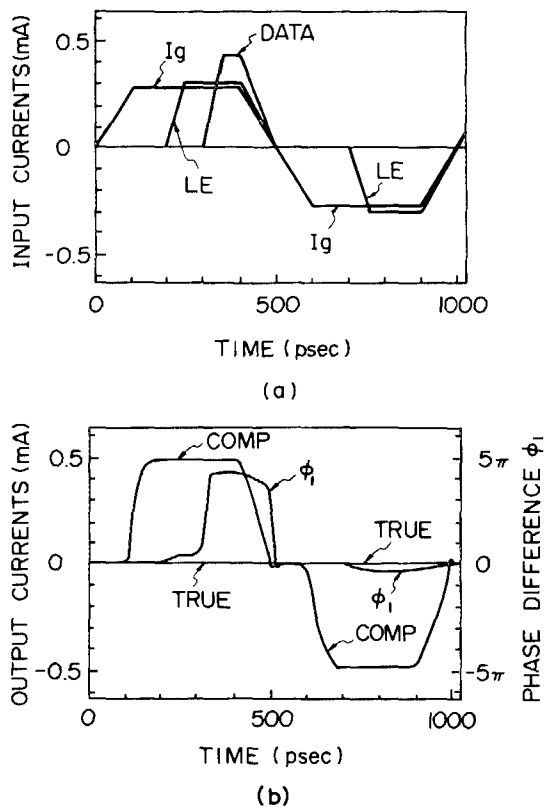


FIG. 8. A two cycle computer simulation of the latch with a damping resistance of  $4.0 \Omega$ . The simulation begins with a zero stored in the latch. (a)  $I_g$ —Gate current for the junction  $J_4$  and the sense gate  $Q_1$ . DATA—Data current. LE—Latch enable current. (b) TRUE, COMP—True and complement output currents of the slave circuit.  $\phi_1$ —Quantum phase difference of the junction  $J_1$ .

lated typical result of proper two-cycle operations. The input DATA sequence is “1,” “0.” The damping resistance  $R_D$  of  $1 \Omega$  and the power supply rise time of 100 ps and the cycle time of 500 ps were chosen for the simulations. The latch enable signal is activated in the middle of the active portion every cycle. The simulation begins with “0” stored in the latch circuit. It can be seen that the latch circuit operates properly as the static design in Sec. II expects.

The circuit with damping resistance  $R_D$  larger than  $4 \Omega$  operated improperly as shown in Fig. 8. The improper operation results from the direct shifts of the operating point from L to O and from Q to R in Fig. 4. As a result, when the power supply is turned off, the operating point moves to H in spite of the application of the data signal, and DATA “0” is read out in the next clock cycle. The critical value of  $4 \Omega$  for the damping resistance hardly depends on the power supply

rise time. The damping resistance of  $1 \Omega$  was chosen in this design to assure the proper operation even if the circuit parameters deviate from the designed values in a practical device.

#### IV. CONCLUSIONS

A new current injection Josephson latch employing a single-flux quantum is proposed. It has a master-slave circuit configuration and operates under the ac power supply. Its main features are the capability of high-speed operation, the smallness of the device size, and the compatibility in circuit design and fabrication processes with the current injection Josephson logic gates. The operation principle and the circuit design have been described in detail, with stress on wider operating margins for various input currents. Finally, dynamical behaviors of the latch circuit have been investigated using computer simulations. The value of the damping resistor assuring the proper operation has been determined from the simulation results. The experimental verifications of this latch including the high-speed capability will be shown in a companion paper.

#### ACKNOWLEDGMENTS

The authors would like to thank J. S. Tsai for his valuable discussions. They also would like to thank Y. Takayama and H. Abe for their continuous encouragement during this work. The present research effort is part of the National Research and Development Program on “Scientific Computing System,” conducted under a program set by the Agency of Industrial Science and Technology, Ministry of International Trade and Industry.

- <sup>1</sup>H. H. Zappe, IEEE Trans. Magn. **MAG-13**, 41 (1977).
- <sup>2</sup>T. Gheewala, Appl. Phys. Lett. **35**, 720 (1979).
- <sup>3</sup>T. A. Fulton, S. S. Pei, and L. N. Dunkelberger, Appl. Phys. Lett. **34**, 709 (1979).
- <sup>4</sup>T. Gheewala and A. Mukherjee, Technical Digest of the International Electron Devices Meeting (IEEE, Piscataway, NJ, 1979), p. 482.
- <sup>5</sup>S. Takada, S. Kosaka, and H. Hayakawa, Jpn. J. Appl. Phys. **19**, 607 (1980).
- <sup>6</sup>K. Hohkawa, M. Okada, and A. Ishida, Appl. Phys. Lett. **39**, 653 (1981).
- <sup>7</sup>J. Sone, T. Yoshida, and H. Abe, Appl. Phys. Lett. **40**, 741 (1982).
- <sup>8</sup>A. Davidson, IEEE J. Solid-State Circuits **SC-13**, 583 (1978).
- <sup>9</sup>H. C. Jones and T. R. Gheewala, IEEE J. Solid-State Circuits **SC-17**, 1201 (1982).
- <sup>10</sup>T. Yamada and J. Sone, J. Appl. Phys. **59**, 3202 (1986).
- <sup>11</sup>M. B. Ketchen, Technical Digest of the International Electron Devices Meeting (IEEE, Piscataway, NJ, 1979), p. 489.
- <sup>12</sup>E. O. Shultz-DuBois and P. Wolf, Appl. Phys. **16**, 317 (1978).
- <sup>13</sup>J. Sone, T. Yoshida, S. Tahara, and H. Abe, Appl. Phys. Lett. **41**, 886 (1982).
- <sup>14</sup>J. H. Greiner, C. J. Kircher, S. P. Klepner, S. K. Lahiri, A. J. Warnecke, S. Basavaiah, E. T. Yen, J. M. Baker, P. R. Brosious, H. W. Huang, M. Murakami, and I. Armes, IBM J. Res. Dev. **24**, 195 (1980).