Current-injection Josephson latch employing a single-flux quantum. II

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A novel current-injection Josephson latch with a single-flux quantum memory is experimentally verified. The experimental latch is fabricated by 5-μm Pb-alloy technology and occupies an area of $270\times175\ \mu m^2$, achieving one order of magnitude area reduction compared to magnetically coupled latch. In low-frequency experiments, the proper operation of a single latch under arbitrary input conditions and the proper data transfer from latch to latch are observed. In high-speed experiments, the proper operation of a single latch with cycle time down to 3.7 ns is observed, which is limited by the high-speed restriction of the test instruments at room temperature. These results show the possibility that the complete current injection logic system can be constructed by combining the present latch and current-injection logic gates.

I. INTRODUCTION

Josephson devices are promising candidates for the high-speed switching devices in the future ultrahigh performance computers. Most Josephson logic gates work in a latching mode.[1,2] These latching gates can be reset to the "off" state (superconducting state) by lowering their power supply current to zero. Thus, in order to store the data during the zero-supply current state, Josephson latch circuits are required to implement the Josephson logic circuits.[3,4]

In a companion paper, the design and the operating principle of a novel current-injection Josephson latch circuit with a single-flux quantum memory have been reported. In this latch, data are stored as a circulating current in a superconducting loop composed of a single Josephson junction and inductances. The stored data are read out by a two-junction interferometer gate directly coupled to the loop.

This paper reports the experimental verifications of the proposed latch. The latch was fabricated by 5-μm Pb-alloy technology and occupied an area of $270\times175\ \mu m^2$, achieving one order of magnitude area reduction compared to a magnetically coupled Josephson latch.[4] In low-frequency functional tests, the proper operation of a single latch under arbitrary input conditions as well as the proper data transfer from latch to latch was verified. In high-speed experiments, the proper operation of a single latch was verified down to 3.7-ns cycle time, limited by the high-frequency restriction of the room temperature test instruments. The latch circuit layout and its fabrication process are presented in Sec. II. The evaluations of the circuit parameters in the fabricated latch and its functional tests are described in Sec. III and the high-speed experiments including the computer simulations in Sec. IV. Conclusions are summarized in Sec. V.

II. LATCH CIRCUIT FABRICATION

The latch circuit configuration is shown in Fig. 1(a) with the designed circuit parameters. Photographs of a single latch and a three-bit serial latch fabricated by standard Pb-alloy fabrication processes[6] are shown in Figs. 1(b) and 1(c), respectively. The Josephson junctions have [Pb-In-Au/oxide/Pb-Bi] sandwich structures. Inductances and transmission lines are designed by 5-μm rule and resistors by 4-μm rule. The smallest Josephson junctions have 5-μm diameters. The layer structure of the fabricated latch is listed in Table I. The storage loop, consisting of a single-junction J_1, inductances L_2 and L_3, and a sense gate Q_1 directly coupled to the loop, occupy an area of $90\times50\ \mu m^2$. The data-signal generator consisting of two OR gates G_1 and G_2 and an AND gate D_1, and the output generator consisting of two OR gates G_3 and G_4 in the slave circuit occupy the rest of the area. The whole latch occupies an area of $270\times175\ \mu m^2$. Compared to the magnetically coupled latch[4] occupying an area of $1000\times300\ \mu m^2$ by 2.5-μm rule, one order of magnitude reduction in the device size is demonstrated.

III. FUNCTIONAL TESTS

A. Circuit parameters

Prior to the functional tests, various circuit parameters in the fabricated latch were evaluated. The critical currents of the junctions in the latch were evaluated by measuring I-V characteristics of serially connected junctions in the test circuit. The measurements showed that the critical currents were about 14% lower than the nominal designed value. The measured critical currents I_1–I_5 for the junctions J_1–J_5 were as follows:

$I_1 = 0.26$ mA (designed to be 0.30 mA),

$I_2 = I_3 = 0.13$ mA (designed to be 0.15 mA),

TABLE I. The layers for the latch fabricated by 5-μm Pb-alloy technology.

Layer	Material	Thickness (nm)	Function
Sub.	Si wafer		Substrate
M_1	Nb	300	Ground plane
I_1	Nb_2O_5	35	Ground insulation
I_2	SiO	150	Ground insulation
C	PbInAu	200	Ground contact
R	$AuIn_2$	40	Resistor
M_2	PbInAu	200	Base electrode
I_3	SiO	270	Junction definition
M_3	PbInAu	600	Interconnection
I_4	PbO/In_2O_5		Tunnel barrier
M_4	PbBi	400	Counter electrode

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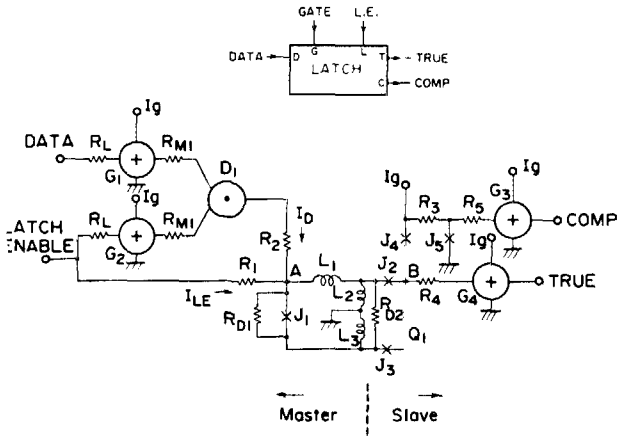
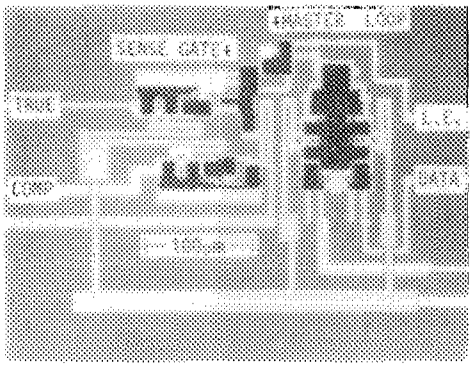


(a)



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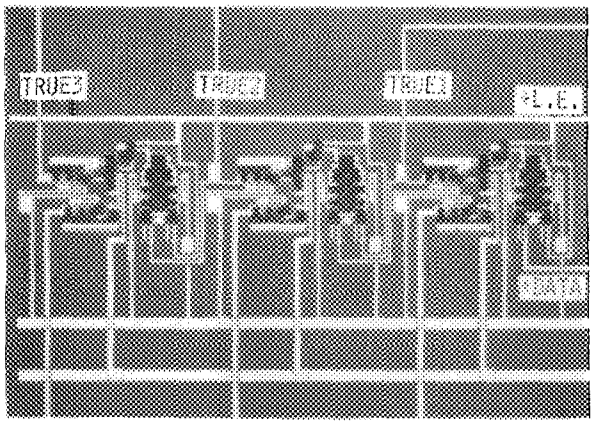
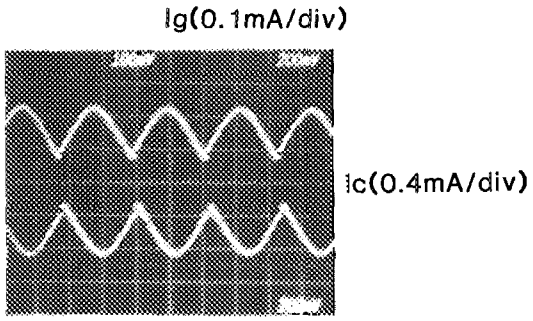


(c)

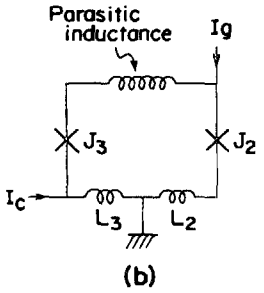
FIG. 1. A current-injection Josephson latch with a single-flux quantum memory. GATE, LE, DATA, TRUE, and COMP represent power supply current, latch enable signal, data signal, true and complement outputs, respectively. (a) The schematic diagram of a novel latch and its symbol. $I_1 = 0.30$ mA, $I_2 = I_3 = 0.15$ mA, $I_4 = I_5 = 0.21$ mA, $L_1 = 5.3$ pH, $L_2 = 2.3$ pH, $R_{D1} = R_{D2} = 1.0\ \Omega$. (b) The photograph of a single latch fabricated by 5 μm Pb-alloy technology. (c) The photograph of a three-bit serial latch.

$I_4 = I_5 = 0.17$ mA (designed to be 0.21 mA).

The resistor values were evaluated by measuring the 50 Ω test patterns on the chip and turned out to be 5% lower than the designed values. However, these resistor value deviations did not cause any improper operations of the latch.



(a)



(b)

FIG. 2. The control characteristics of the sense gate Q_1. I_g and I_c represent threshold gate current and control current, respectively. (a) The photograph of measured I_g plotted as a function of I_c. (b) The schematic diagram of a test circuit with a parasitic inductance isolated from the storage loop.

The inductance values of L_2 and L_3 were evaluated by investigating the control characteristics of the sense gate Q_1. The measured threshold gate current plotted as a function of the control current is presented with a test circuit configuration in Figs. 2(a) and 2(b). Figure 2(a) shows that the control characteristic curve repeats with the control current period of 0.90 mA. Thus, the inductances L_2 and L_3 can be estimated to have a value of 2.3 pH, realizing the designed value properly. The slight asymmetry in the characteristic curve is attributed to a parasitic inductance of 1.7 pH arising from the counter electrode pattern connecting the junctions and the inductances. This parasitic inductance is schematically shown in the equivalent test circuit diagram in Fig. 2(b).

Because of this parasitic inductance, there was the possibility that the characteristics of the sense gate Q_1 suffered a modification from the designed one. The characteristics of the sense gate Q_1 coupled to a storage loop are calculated using measured circuit parameters. The threshold gate current is plotted as a function of the quantum phase difference of the junction J_3 in Fig. 3: (a) in the presence of the parasitic inductance and (b) in the absence of the parasitic inductance. The solid lines represent the thermodynamically stable regions and the broken lines represent the unstable regions. When the data "0" is stored in the storage loop, the operating point moves from S to S' or S'' as the gate current rises in the next cycle. For the gate current having an amplitude larger than that of the current corresponding to S' or S'', the sense gate switches to the resistive state. When the data "1" is stored during the positive cycle, the operating point moves from T to T'', while when the data "1" is stored during the negative cycle, the operating point moves from U to U' as the gate current rises in the next cycle. For the gate

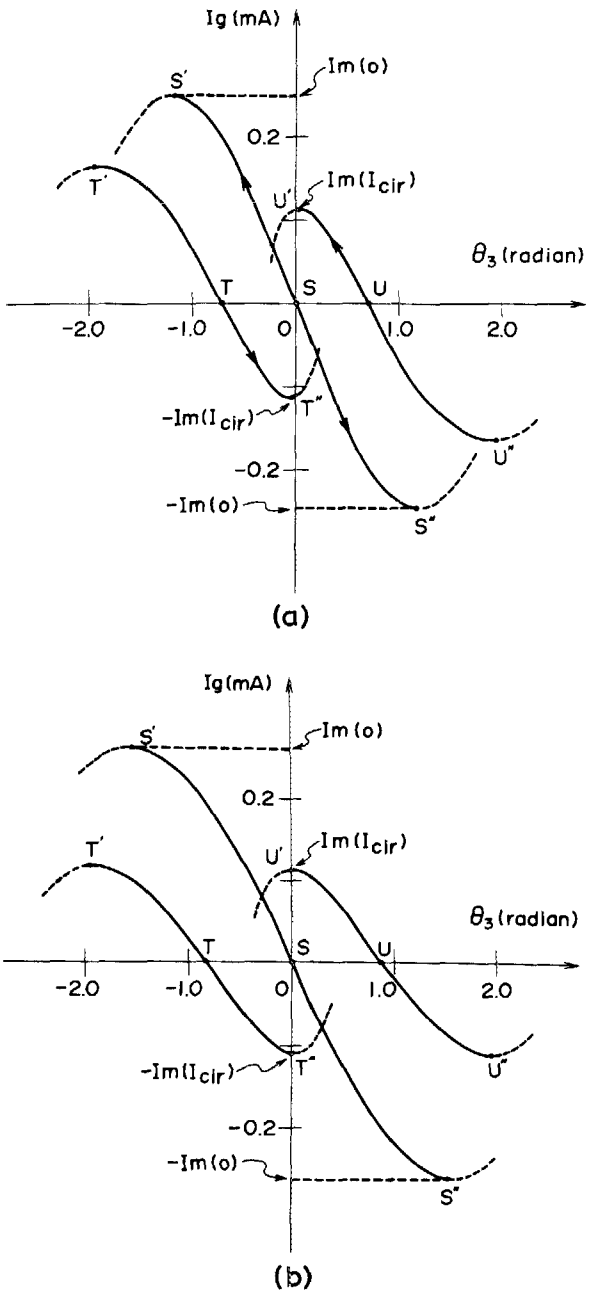


FIG. 3. The characteristics of the sense gate Q_1 having a storage loop calculated using measured circuit parameters: (a) in the presence of a parasitic inductance and (b) in the absence of a parasitic inductance. The threshold gate current I_g is plotted as a function of the quantum phase difference θ_3 of the junction J_3. The solid lines represent the thermodynamically stable regions and the broken lines represent the unstable regions.

current having an amplitude larger than that of the current corresponding to T'' or U', the sense gate switches. Thus, the threshold gate current magnitude is $I_m(0)$ when the data "0" is stored and $I_m(I_{cir})$ when the data "1" is stored. Figures 3(a) and 3(b) show that even in the presence of the parasitic inductance of 1.7 pH, the values of $I_m(0)$ and $I_m(I_{cir})$ are almost the same as those in the absence of the parasitic inductance. Therefore, the present latch does not suffer a serious read-out margin reduction despite the presence of the parasitic inductance. On the contrary, if the power line of the gate current were connected between the junction J_3 and the parasitic inductance, the operating points would move to T' or U'' when the data "1" is stored as the gate current rises. Therefore, $I_m(I_{cir})$ would become larger, resulting in a significant read-out margin reduction.

The inductance value of L_1 was estimated by measuring a latch enable current margin defined by the value $\pm (I_{max} - I_{min})/(I_{max} + I_{min})$, where I_{max} implied the maximum latch enable current not to cause a circulating current to enter the storage loop in the absence of a data signal and I_{min} implied the minimum latch enable current required to reset the loop in the absence of a data signal. This margin was a function of the inductances L_1-L_3 and the critical currents I_1-I_3. Therefore, the inductance value of L_1 could be calculated from the measured latch enable current margin and the measured parameters L_2, L_3, and I_1-I_3.[5] Since the latch enable signal margin of the fabricated latch was measured to be $\pm$ 45%, the inductance value of L_1 was calculated to be 5.3 pH. Although the products of the inductance values L_1-L_3 and the critical currents I_1-I_3 becomes about 15% lower than the designed value, the latch operates properly as expected in the circuit design except for the slight deviations in the various input current margins.

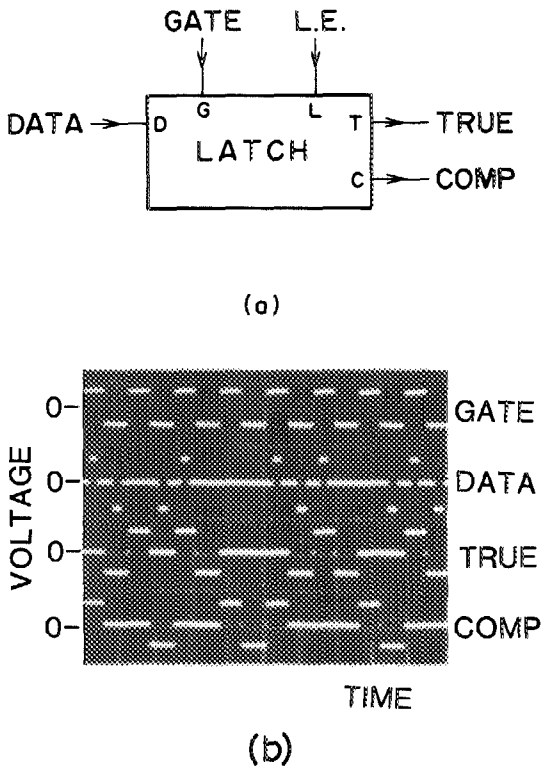


FIG. 4. The one-bit latch experiments. GATE, DATA, TRUE, and COMP represent power supply current, data signal, true and complement outputs, respectively. The latch is powered by a bipolar trapezoidal current. The logical value "0" is represented by a zero-voltage state and the logical value "1" by a voltage state. The true output "1" is generated only when the data-signal "1" is applied during the last cycle, while the complement output is generated only when the data-signal "0" is applied during the last cycle. (a) The schematic circuit diagram of the experiments. (b) The operation photograph of a one-bit latch.

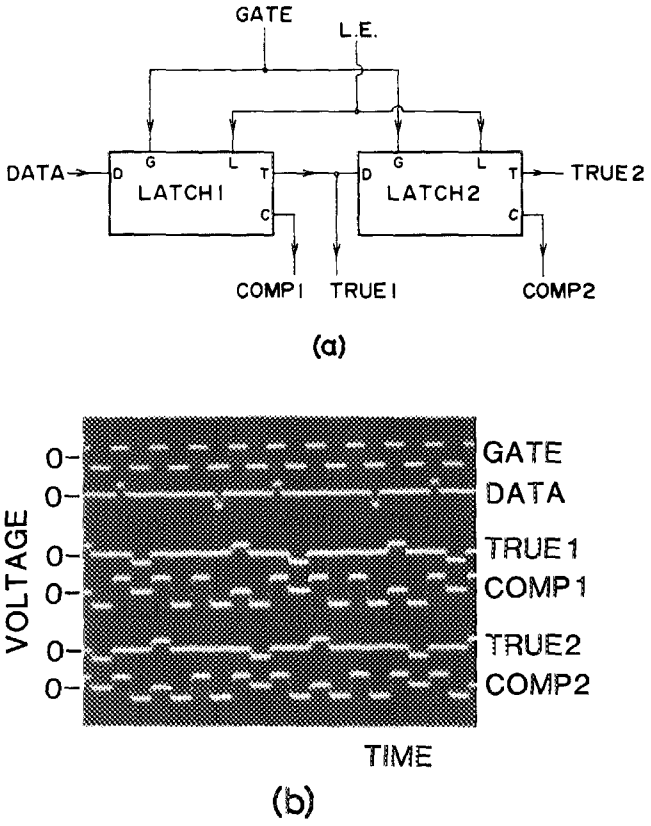


FIG. 5. The two-bit serial latch experiments. GATE, DATA, and TRUE (COMP) 1,2, represent power supply current, input data to the 1st latch, and the true (complement) output of the 1st or 2nd latch, respectively. The true output is generated only when the data-signal "1" is applied during the last cycle, while the complement output is generated only when the data signal "0" is applied during the last cycle. The proper data transfer from latch to latch is shown. (a) The schematic circuit diagram of the experiments. (b) The operation photograph of the two-bit latch with true and complement outputs.

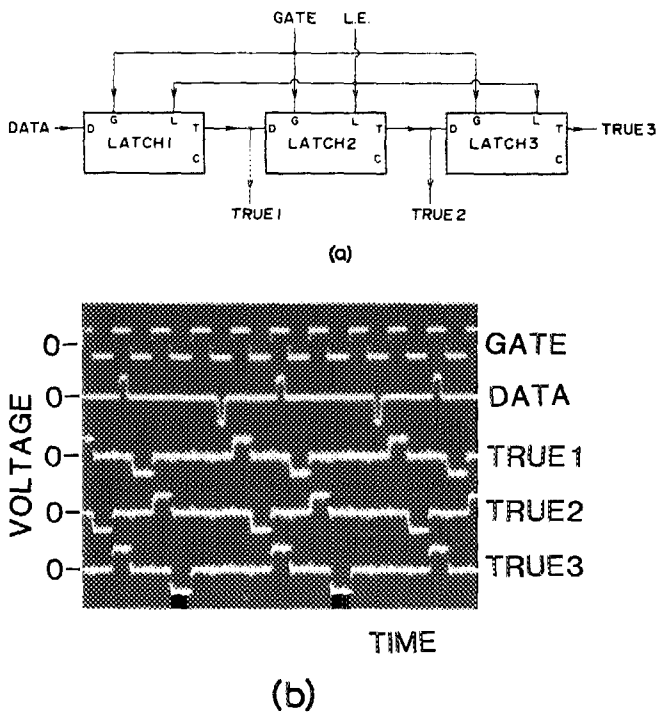


FIG. 6. The three-bit serial latch experiments. GATE, DATA, and TRUE1-3 represent power supply current, input data to the 1st latch, the true outputs of first to the third latch, respectively. The true output is generated only when the data-signal "1" is applied during the last cycle. The proper data transfer from latch to latch is shown. (a) The schematic circuit diagram of the experiments. (b) The operation photograph of the three-bit latch with each true output.

B. One-bit latch experiments

The one-bit latch operation has been experimentally measured under arbitrary input conditions. The latch was powered by a bipolar trapezoidal current. The latch enable signal and the data signal applied to the latch were also bipolar. Thus, the logical value of "0" was represented by a zero-voltage state and the logical value "1" by a voltage state. The experimental latch operation is shown in Figs. 4(a) and 4(b). The true output "1" is generated only when the data signal "1" is applied during the last cycle, while the complement output is generated only when the data signal "0" is applied during the last cycle. These results indicate the proper operation of the experimental latch.

The operating windows for various input currents were measured. The window for the gate currents (power supply currents) fed to four OR gates was 0.85 mA $\pm$ 7% (designed to be 42%), the window for the latch enable signal applied to both the OR gate and the storage loop was 0.50 mA $\pm$ 45% (designed to be 38%) and the window for the gate current powering the Josephson junction J_4 and the gate Q_1 was 0.30 mA $\pm$ 25% (designed to be 33%). The latch enable signal and the gate current for the junction J_4 and the sense gate Q_1 have almost the same margins as designed. Thus, the latch was regarded to operate as expected by the design. The gate current powering the OR gates contained in the data-signal generator and the output generators had a significantly smaller margin than the designed one. The reason for the decrease in the gate current margin could be attributed to the scatterings in the circuit parameters, especially those of the Josephson critical currents.

C. Shift register experiments

In shift register experiments, true and complement outputs were observed in a two-bit serial latch experiment and true outputs were observed in a three-bit serial latch experiment. Schematic circuit diagrams and measured bit-pattern photographs for these latches are shown in Figs. 5(a), 5(b), Figs. 6(a), and 6(b). In these figures, the true output is generated only when the data-signal "1" is applied during the last cycle. In Fig. 5(b), the complement output is generated only when the data-signal "0" is applied during the last cycle. The proper data transfer from latch to latch has been verified by these experiments.

Current margins for the three-bit latch became considerably worse than those for the one-bit latch. The gate current margin for the OR gates was $\pm$ 1%, the gate current margin for the junction J_4 and the sense gate Q_1 was $\pm$ 14%, and the gate current margin for the sense gate Q_1 was $\pm$ 7%. These decreases in margins were considered to be due to the scatterings in circuit parameters over the experimental chip,

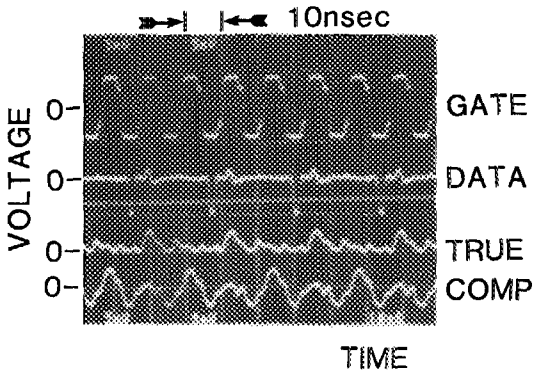


FIG. 7. The high-speed operation of a latch at 6-ns cycle time. GATE, DATA, TRUE, and COMP represent power supply current, data signal, true and complement outputs, respectively. The input data sequence 0, 0, 1, 0 is applied to the latch. The true output 0, 0, 0, 1 and the complement output 1, 1, 1, 0 are generated.

especially those of Josephson critical currents.

IV. HIGH-SPEED OPERATION EXPERIMENTS

The high-speed operation experiments of the one-bit latch was carried out with the input data sequence 0, 0, 1, 0. A bipolar trapezoidal current fed from a HP8091A 1-GHz pulser was used for the gate current powering the OR gates and the sense gate Q_1. The pulse generated by another HP8091A pulser was adopted for the latch enable signal. The data signal was activated every four cycles of the gate current, using a quarter prescalar and the HP8091A pulser.

In order to lessen the deterioration of the signal-to-noise ratio due to a large crosstalk noticeable in the high-frequency operation, the following two measures on a chip holder were carried out: (1) Semirigid coaxial cables were adopted for I/O lines connecting the chip holder at liquid-helium temperature and the measurement instruments at room temperature. The adoption of the semirigid coaxial cables enabled the good ground contact between the chip holder and the cables and achieved the satisfactory shielding of the inner conductors. (2) The I/O strip lines in the chip holder having (ground/10 μm thickness polymer/center conductor/100 μm thickness polymer/ground) sandwich structures connected the pads on the chip and the semirigid coaxial cables mentioned above. The strip lines had 50-μm line and space and 5 mm length. Because of the thin polymer insulation layer adopted, the fringing electromagnetic field was suppressed and the crosstalk among the strip lines was considerably reduced.

Because of the very fast cycle time, the adjustment of the phases among the gate currents, the latch enable signal, and the data signal was of crucial importance. Particularly, the latch enable current had to be applied after the rise of the gate current. The I/O lines connecting the chip at liquid-helium temperature and the output terminals at room temperature were adjusted in length so that their delay time differences were less than 0.1 ns.

The high-speed operation at 6-ns cycle time is shown in Fig. 7. The true output is generated only when the data-

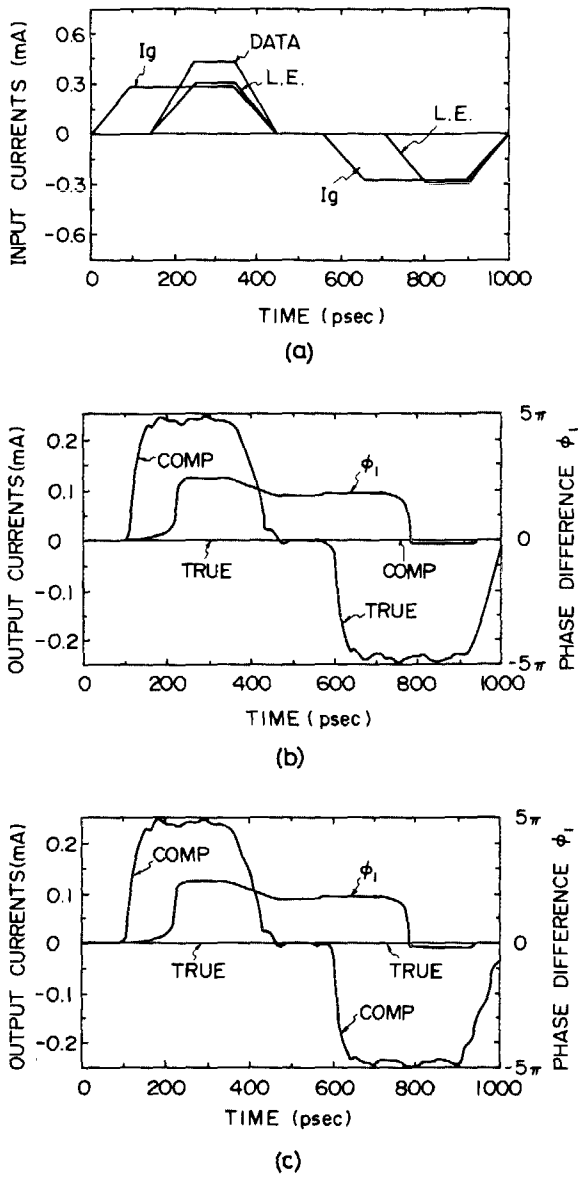


FIG. 8. Computer simulation results. The power supply waveform with a dead time of 100 ps is applied to the latch. (a) The input current waveforms. GATE, LE, and DATA denote power supply current, latch enable signal, and data signal, respectively. (b) The proper operation with a rise time of 30 ps. TRUE, COMP, and ϕ_1, represent true, complement outputs, and the quantum phase difference of the junction J_1, respectively. (c) The erroneous operation with a rise time of 20 ps.

signal "1" is applied during the last cycle while the complement output is generated only when the data signal "0" is applied during the last cycle. These results indicate the proper operation of the latch.

The proper latch operation was observed down to 3.7-ns cycle time, limited not by the high-speed operation capability of the latch itself, but that of the test instruments. Since the current was directly fed to the latch from the test instruments and not regulated by a Josephson regulator,[7] the power supply current became unregulated and nearly sinusoidal at a faster cycle time and adjusting the phase among the input currents was difficult, resulting in the improper operation with a cycle time less then 3.7 ns.

The shortest power supply rise time for the latch to operate properly has been investigated by computer simula-

tions. Punch through phenomena[8,9] in the RCJL gates[2] and the sense gate Q_1 primarily limit the high-speed operation of the latch with the power supply current waveform as shown in Figs. 8(a)–8(c). The power supply current waveform with a dead time of 100 ps shown in Fig. 8(a) was used for simulations to study the intrinsic shortest rise time for the proper latch operation with the punch through phenomena suppressed. The proper operation was maintained with a power supply rise time up to 25 ps as shown in Fig. 8(b). With a rise time faster than 25 ps, the Josephson junction J_4 switched before the sense gate Q_1 in the reading process of the data "1." This was because the sense gate Q_1 had longer turn-on delay than the Josephson junction J_4.[10] The corresponding simulation results are shown in Fig. 8(c).

V. CONCLUSIONS

The proper operations of the novel current-injection Josephson latch circuit with a single-flux quantum memory are experimentally verified. The latch occupies an area of $270\times175\ \mu m^2$, achieving one order of magnitude area reduction compared to a magnetically coupled latch. In low-frequency experiments, the proper operation of a single latch under arbitrary input conditions and the proper data transfer from latch to latch are verified. In high-speed experiments, the proper operation of the single latch is observed down to 3.7-ns cycle time, limited by the high-speed restriction of the test instruments. Computer simulations show that the latch can operate properly down to 25-ps rise time.

These results show the possibility that the complete current injection logic system can be constructed by combining the present latch and current injection logic gates.

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