STRIPED CHANNEL FIELD EFFECT TRANSISTORS WITH A MODULATION DOPED STRUCTURE

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ABSTRACT

We report the fabrication and performance of the striped channel field effect transistor, which consists of a multiple number of narrow channels fabricated on a modulation-doped heterostructure. The two-dimensional squeezing of the conducting channel by applying gate voltage has been confirmed from the channel width dependence of the drain current. By reducing the channel width of the fabricated 0.25μm gate-length striped channel devices, we have observed an enhancement in transconductance as well as improved high frequency performances. Furthermore, more than 3 times improvement in the maximum transconductance has been obtained when the device is cooled to 77K. We interpret these results based on the improved charge controllability due to the channel squeezing effect as well as on the excellent electron transport properties of ultrafine channels.

I. INTRODUCTION

One-dimensional electron systems have attracted considerable interest because of their great potential for ultrahigh speed device applications. Up to present, a number of theoretical analyses have been made to understand the fundamental physics of the one-dimensional electron transport [1-3]. In recent years, several experimental results regarding the transport properties in a quasi one-dimensional structure have been demonstrated employing advanced crystal growth and nanometer scale fabrication technologies [4-5]. Improved transport properties that can be ascribed to characteristic phenomena in the quasi one-dimensional channel have been observed in the low-field characteristics for long-channel devices [4-5]. However, there have been no experiments reported on the high-field behavior of short gate-length FET's with quasi one-dimensional channels.

The striped channel field effect transistor has a multiple number of very narrow parallel channels that run from source to drain. The FET structure is similar to that for the castellated gate MESFET [6] and the Focused-Ion-Striped Transistor (FIST)[7]. In these reported FET's, however, the enhancement in transconductance has been achieved only through the channel wrapping effect, in which the size of the depletion layer is controlled from both vertical and lateral directions. Since the striped channel FET consists of quasi one-dimensional channels fabricated on selectively-doped AlGaAs/GaAs heterostructures, improved electron transport properties can also be expected in addition to the improved charge controllability due to the channel wrapping effect.

In this paper, we report on the fabrication and characteristics of striped channel field effect transistors at room temperature and at liquid-N_2 temperature. Also, transport properties of quasi one-dimensional structures are discussed.

II. DEVICE STRUCTURE AND FABRICATION

The devices were fabricated on selectively-doped AlGaAs/GaAs heterostructures. The layers used in this work consist of an undoped GaAs channel layer, a thin undoped AlGaAs spacer layer, a 200Å AlGaAs layer Si-doped to $2.5 \times 10^{18}cm^{-3}$ and finally a GaAs cap layer also Si-doped to $2.5 \times 10^{18}cm^{-3}$, sequentially grown by MBE on a (100) semi-insulating GaAs substrate. The Al-mole fraction in the highly doped $Al_xGa_{1-x}As$ is 0.3.

Figure 1 schematically illustrates a top view and a cross section of the striped channel FET device. Electron beam lithography was employed for striped channel mesa and

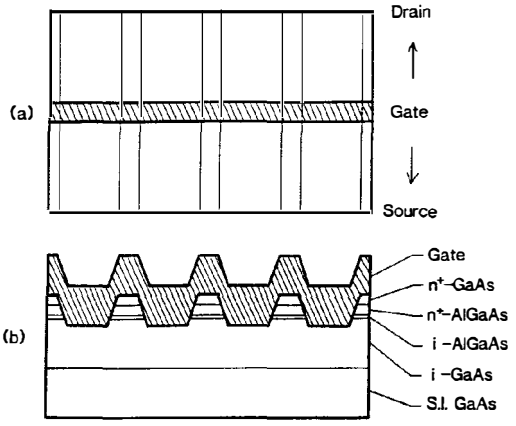

Fig.1 Top view (a) and cross section (b) of striped channel FET.

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gate definitions. Except for the striped channel fabrication step, the device fabrication is based on a conventional mesa-isolated lift- off technology, which is briefly described as follows: Striped channels were delineated by direct write electron beam lithography. AuGe/Ni/Au ohmic contacts were then formed to the source and drain and alloyed in H_2 gas. After the gate level patterning, the GaAs gate area was recessed using wet chemical etching to achieve the desired full channel current. Ti/Al metal layers were then evaporated to form Schottky gates with a triangular cross section using a lift-off technique.

The fabricated device has a 0.25μm gate length with various single channel widths ranging from 0.1 to 1.2μm. Figure 2 is a typical SEM photograph showing a 0.25μm gate length striped channel FET with 0.10μm individual single channel widths. For comparison, conventional two-dimensional electron gas FET's (2DEGFET's) with a 200μm channel width were also fabricated on the same wafer.

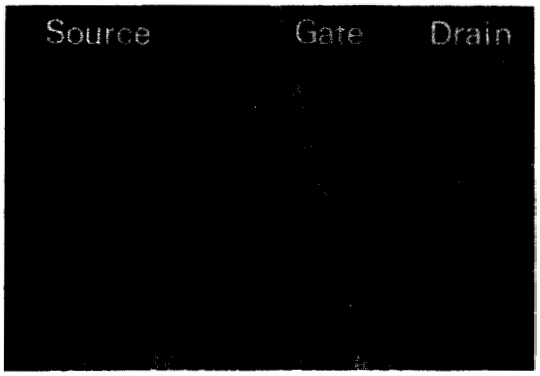

Fig.2 SEM photograph of striped channel FET.

III. DEVICE CHARACTERISTICS AND DISCUSSION

Figure 3 shows plots of drain conductance per channel as a function of the single channel width. The drain conductance is estimated in the low-field linear region (V_{ds}=0.05V). With increasing the single channel width, the drain conductance linearly increases. The intersection of the extrapolated line with the horizontal axis corresponds to the sum of the thicknesses for the lateral depletion layers extending from both sides of the narrow channel. It is obvious that decreasing the gate voltage leads to an increase in the lateral depletion thickness. This result indicates direct evidence regarding the two-dimensional channel squeezing effect in the striped channel FET structure.

At a sufficiently large drain voltage, the saturated drain current of the striped channel FET can be written as

$$I_{ds} = qn_s v_s N W_{sc} \tag{1}$$

where q is the electronic charge, n_s is the sheet carrier density, v_s is the electron velocity, N is the number of striped channels and W_{sc} is the single channel width. The transconductance, g_m, is the first derivative of the drain current with respect to gate voltage. This gives the following expression.

$$g_m = qv_s N W_{sc} \frac{\partial n_s}{\partial V_{gs}} + qv_s n_s N \frac{\partial W_{sc}}{\partial V_{gs}} \tag{2}$$

The second term in Eq.(2) is important for the striped channel device, while it is negligible for conventional FETs. To estimate the difference in transconductance among devices with various single channel widths, the value of g_m/I_{ds} is calculated:

$$\frac{g_m}{I_{ds}} = \frac{1}{qn_s v_s} \cdot \frac{g_m}{NW_{sc}} \tag{3}$$

Since n_s and v_s are assumed to be independent of W_{sc} for a given V_{gs} value, the calculated g_m/I_{ds} value is proportional to $g_m/(NW_{sc})$, i.e., the normalized g_m, which is estimated from the measured g_m value divided by the total gate width. Figure 4 shows plots of g_m/I_{ds} as a function of the gate voltage for devices with various single channel widths. Values are estimated at V_{ds}=2.0V. Over the whole V_g values investigated, the g_m/I_{ds} value increases with decreasing the single channel width. This indicates a larger $g_m/(NW_{sc})$ value is obtained for the device having a shorter single channel width. From the results shown in Figs. 3 and 4, it is concluded that the striped channel FET structure gives an improvement in charge controllability due to the two-dimensional squeezing effect.

In order to establish a better understanding of electron transport in the striped channel FET, device characteristics were also measured at 77K under conditions of white illumination. Typical DC characteristics are shown in Fig.5. The device has a 0.25μm gate-length with 133 single channels of 0.10μm width. We can clearly see an enhancement in both transconductance and saturated drain current by cooling the

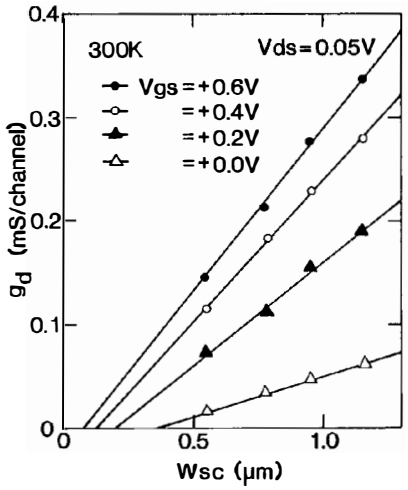

Fig.3 Drain conductance of striped channel FET's as a function of the single channel width for various gate voltages at V_d=0.05V.

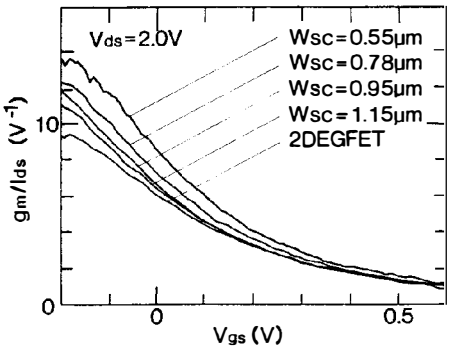

Fig.4 g_m/I_d, versus gate-source voltage of striped channel FET's

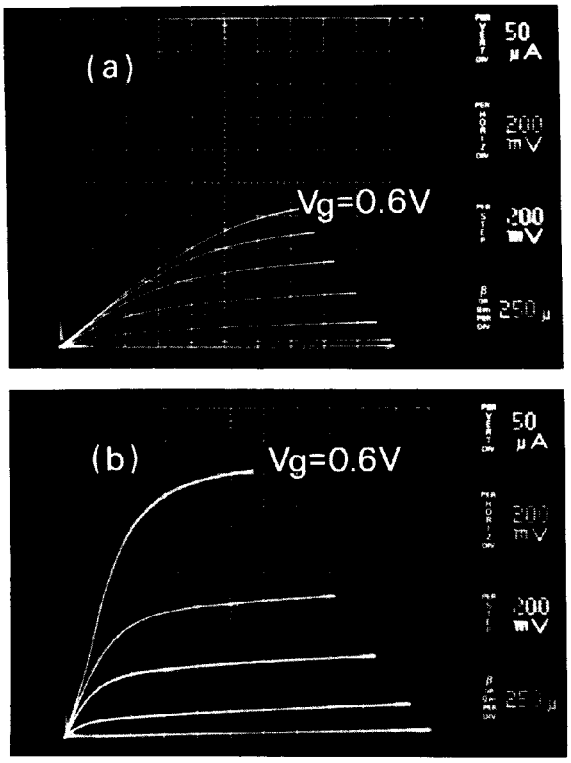

Fig.5 I-V characteristics of 0.25μm gate-length striped channel FET with single channel width of 0.10μm (a) at 300K and (b) at 77K.

device down to 77K. The drain conductance in the linear region is improved by a factor of more than 4. In Fig.6, the ratio of maximum transconductances measured at 77K and 300K, $g_m(77K)/g_m(300K)$, as a function of drain voltage is shown for the devices with various single channel widths. The $g_m(77K)/g_m(300K)$ factor increases with the decrease in single channel width. In the low-field region (V_d, <0.5V), transconductance is improved by a factor of 3-5. An interesting point here is the 2-3 times greater enhancement in transconductance observed in the drain saturated region. For the conventional 2DEGFET made on the same wafer, the improvement factor in the saturated region is only 1.3, which is consistent with the results reported by Duh et al [8]. These results suggest the improved high-field transport properties, such as enhanced electron velocity, of quasi one-dimensional structures at 77K.

S-parameters are measured for 0.25μm gate-length devices with single channel width of 0.59, 0.29 and 0.18μm. Using the measured S-parameters, current gains are calculated versus frequencies. Results are shown in Fig.7. The cut-

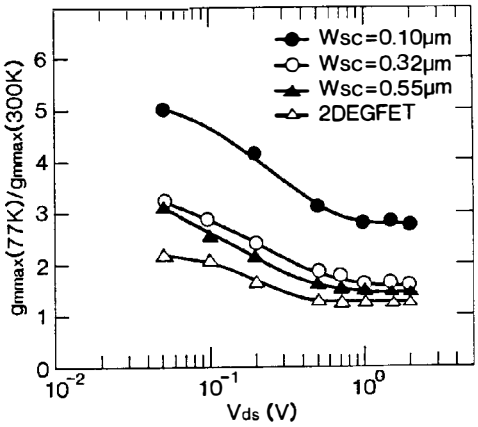

Fig.6 $g_{mmax}(77K)/g_{mmax}(300K)$ versus drain voltage for various single channel widths.

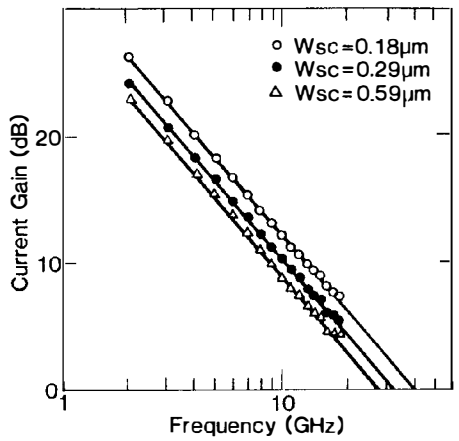

Fig.7 Current gain versus frequency for 0.25μm gate-length striped channel FET's.

off frequencies of these FET's with 0.59μm, 0.29μm and 0.18μm channel widths are estimated to be 28GHz, 33GHz and 40GHz respectively. It is obvious that the FET with a narrower single striped channel gives a higher cut-off frequency. These high frequency results suggest the possibility of improved high-field transport properties, in addition to the improved charge controllability, in the narrower striped channel structure even at room temperature since these data are taken in a drain saturated region (V_{ds} =1.5V).

IV. CONCLUSION

We have described the fabrication and characteristics of striped channel field effect transistors. In the striped channel FET's, enhanced transconductances as well as higher cut-off frequencies have been obtained with decreasing the width of the single channel. More than 3 times enhancement in transconductance has been obtained by cooling the device from room temperature to 77K. The improvements in the device performances can be explained based on the channel squeezing effect of the corrugated gate structure as well as on the excellent electron transport properties of ultrafine channels even at high electric fields.

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