

Personal Information

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Assistant professor at the Computer Engineering Department at University of California, Santa Cruz.

Education

- 2004** Ph.D. Computer Science, University of Illinois at Urbana Champaign.
- 1999** M.S. Computer Science, University of Illinois at Urbana Champaign.
- 1997** M.S. Computer Engineering, Ramon Llull University (Spain)
- 1994** B.S. Computer Science, Ramon Llull University (Spain)

Awards and Funding

- 2009, SUN cash gift (\$75K)
- 2008, NVIDIA cash gift (\$70K)
- 2008, PI NSF CRI: IAD Temperature Measurement Infrastructure for Power, Variability, and Reliability Analysis (\$275K)
- 2007, PI NSF SMA: Accurate Temperature Measurement Infrastructure and Methodology for Power, Variability, and Reliability Analysis. (co-PI are Ali Shakouri, Matthew Gutthaus, Steve Kang, and Michael Huang) (\$300k UCSC + \$100k Rochester)
- 2007, PI NASA/UARC, *Radiation Tolerant FPGA Processor* (\$25k)
- 2007, SUN Academic Excellence Award (\$110K)
- 2007, co-PI Special Research Grant from UCSC (PI is Matthew Gutthaus) (\$20k)
- 2007, Xilinx University Donation Software (\$8k)
- 2006, co-PI IES Berkeley/France Fund Award (co-PI is Albert Cohen) (\$9k)
- 2006, PI Special Research Grant from UCSC (\$12k)
- 2006, PI NASA/UARC (\$50k) *Checkpointed Fault Tolerant FPGA Systems*
- 2006, PI NSF CAREER (\$400k) *Understanding, Estimating, and Reducing Processor Design Complexity*
- 2006, SUN equipment (Niagara server \$16k)
- 2006, Altera equipment (Stratix II DSP board \$5k)
- 2006, IEEE Micro Top Picks in Computer Architecture
- 2005, PI DARPA PERCS subcontract (\$20k)
- 2003, IBM Graduate Research Fellowship
- 2003, J. Poppelbaum Memorial Award, University of Illinois

Recent Selected Publications

Conferences

- [1] *Processor Verification with hwBugHunt*, Sangeetha Sudhakarishnan, Liying Su, and Jose Renau, IEEE International Symposium on Quality Electronic Design (**ISQED**), March 2008.
- [2] *Effective Optimistic-Checker Tandem Core Design Through Architectural Pruning*, Francisco J. Mesa-Martinez and Jose Renau, 40th International Symposium on Microarchitecture (**MICRO**), December 2007.
- [3] *Power Model Validation Through Thermal Measurements*, Francisco J. Mesa-Martines, Joseph Nayfach-Battilan, and Jose Renau, 34th International Symposium on Computer Architecture (**ISCA**), June 2007.

- [4] *SEED: Scalable, Efficient Enforcement of Dependences*, Francisco J. Mesa-Martinez, Michael C.Huang, and Jose Renau, 15th International Conference on Parallel Architectures and Compilation Techniques (**PACT**), September 2006.
- [5] *uComplexity: Estimating Processor Design Effort*, Cyrus Bazeghi, Francisco J. Mesa-Martinez, and Jose Renau. 38th International Symposium on Microarchitecture (**MICRO**), November 2005.

Students

- Phd: Carlos Cabrera (2005-), Sangeetha Nair (2005-), Michael Brown (2006-), Wael Ashmawi (2006-), Alamelu Sankaranarayanan (2007-), David Munday (2007-), Rigo Dicochea (2007-), Madan Das (2008-), Ehsan Ardestani (2008-), Gabriel Southern (2008-), Elnaz Ebrahimi (2009-)
- MS: Anupam Garg (2007-), Gregory Jackson (2009-), Tom Golubev (2009-)

Graduated:

- PhD: Javi Martinez (2004-07), Cyrus Bazeghi (2004-08)
- MS: Shantanu Kale (2005-06), Liying Su (2005-06), David Brian Van Der Bokke (2005-06), Suraj Narender (2005-07), Angela Schmid (2006-07), Matt Fischler (2006-07), Melisa Nuñez (2005-08), Joseph Nayfach (2005-08), Keertika Singh (2008-09)

Publications

Conferences

- [1] *SOI, Interconnect, Package, and Mainboard Thermal Characterization*, Joseph Nayfach-Battilana and Jose Renau, Poster with proceedings at International Symposium on Low Power Electronics and Design (**ISLPED**), August 2009.
- [2] *Measuring and Modeling Variability using Low-Cost FPGAs*, Michael Brown, Cyrus Bazeghi, Matthew Guthaus and Jose Renau, Poster with Proceedings at the International Symposium on Field-Programmable Gate Arrays (**FPGA**), February 2009.
- [3] *Processor Verification with hwBugHunt*, Sangeetha Sudhakarishnan, Liying Su, and Jose Renau, IEEE International Symposium on Quality Electronic Design (**ISQED**), March 2008.
- [4] *Effective Optimistic-Checker Tandem Core Design Through Architectural Pruning*, Francisco J. Mesa-Martinez and Jose Renau, 40th International Symposium on Microarchitecture (**MICRO**), December 2007.
- [5] *Estimating Design Time for System Circuits*, Cyrus Bazeghi Francisco J. Mesa-Martinez, Brian Greskamp, Josep Torrellas, and Jose Renau, 15th IFIP International Conference on Very Large Scale Integration (**VLSI-SoC**), October 2007.
- [6] *Power Model Validation Through Thermal Measurements*, Francisco J. Mesa-Martines, Joseph Nayfach-Battilan, and Jose Renau, 34th International Symposium on Computer Architecture (**ISCA**), June 2007.
- [7] *SEED: Scalable, Efficient Enforcement of Dependences*, Francisco J. Mesa-Martinez, Michael C.Huang, and Jose Renau, 15th International Conference on Parallel Architectures and Compilation Techniques (**PACT**), September 2006.
- [8] *POSH: A TLS Compiler that Exploits Program Structure*, Wei Liu, James Tuck, Luis Ceze, Wonsun Ahn, Karin Strauss, Jose Renau and Josep Torrellas, ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (**PPoPP**), March 2006.
- [9] *uComplexity: Estimating Processor Design Effort*, Cyrus Bazeghi, Francisco J. Mesa-Martinez, and Jose Renau. 38th International Symposium on Microarchitecture (**MICRO**), November 2005.

- [10] *POSH: A Profiler-Enhanced TLS Compiler that Leverages Program Structure*, Wei Liu, James Tuck, Luis Ceze, Karin Strauss, Jose Renau, and Josep Torrellas. The Second Watson Conference on Interaction between Architecture, Circuits, and Compilers (**P=AC2**), September 2005.
- [11] *Thread-Level Speculation on a CMP Can Be Energy Efficient*, Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti Sarangi, James Tuck, and Josep Torrellas. International Conference on Supercomputing (**ICS**), June 2005.
- [12] *Tasking with Out-of-Order Spawn in TLS Chip Multiprocessors: Microarchitecture and Compilation*, Jose Renau, James Tuck, Wei Liu, Luis Ceze, Karin Strauss, and Josep Torrellas. International Conference on Supercomputing (**ICS**), June 2005.
- [13] *Programming the FlexRAM Parallel Intelligent Memory System*, Basilio Fraguera, Jose Renau, Paul Feautrier, David Padua, and Josep Torrellas, International Symposium on Principles and Practice of Parallel Programming (**PPoPP**), June 2003.
- [14] *Positional Adaptation of Processors: Application to Energy Reduction*, Michael Huang, Jose Renau, and Josep Torrellas, International Symposium on Computer Architecture (**ISCA**), June 2003.
- [15] *Cherry: Checkpointed Early Resource Recycling in Out-of-order Microprocessors*, José F. Martínez, Jose Renau, Michael Huang, Milos Prvulovic, and Josep Torrellas, International Symposium on Microarchitecture (**MICRO**), November 2002.
- [16] *Energy-Efficient Hybrid Wakeup Logic*, Michael Huang, Jose Renau, and Josep Torrellas, International Symposium on Low Power Electronics and Design (**ISLPED**), August 2002.
- [17] *Cache Decomposition for Energy-Efficient Processors*, Michael Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, International Symposium on Low Power Electronics and Design (**ISLPED**), August 2001.
- [18] *A Framework for Dynamic Energy Efficiency and Temperature Management*, Wei Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, International Symposium on Microarchitecture (**MICRO**), December 2000.

Journals

- [1] *Using Checkpoint-Assisted Value Prediction to Hide L2 Misses*, Luis Ceze, Karin Strauss, James Tuck, Jose Renau, and Josep Torrellas, ACM's Transactions on Architecture and Code Optimization (**TACO**), March 2006.
- [2] *Energy-Efficient Thread-Level Speculation on a CMP*, Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti Sarangi, James Tuck, and Josep Torrellas. IEEE Micro Special Issue: **Micro's Top Picks** from Computer Architecture Conferences, January-February 2006.
- [3] *CAVA: Hiding L2 Misses with Checkpoint-Assisted Value Prediction*, Luis Ceze, Karin Strauss, James Tuck, Jose Renau, and Josep Torrellas, IEEE TCCA Computer Architecture Letters (**TCCA**), December 2004.
- [4] *Managing Multiple Low-Power Adaptation Techniques: The Positional Approach*, Michael Huang, Jose Renau, Josep Torrellas, Sidebar, IEEE **Computer Magazine**, December 2003.
- [5] *A Framework for Dynamic Energy Efficiency and Temperature Management*, Wei Huang, Jose Renau, and Josep Torrellas, Journal on Instruction Level Parallelism (**JILP**), October 2001.

Workshops

- [1] *Measuring and Modeling Variability using Low-Cost FPGAs*, Michael Brown, Cyrus Bazeghi, Matthew R. Gutthaus, and Jose Renau, Workshop on Modeling, Benchmarking and Simulation (MOBS), held in conjunction with ISCA-36, June 2009.
- [2] *Implementation of a Power Efficient High Performance FPU for SCOORE*, Wael Ali Ashmawi, John Burr, Abhishek Sharma, Jose Renau, Workshop on Architectural Research Prototyping (WARP) held in conjunction with ISCA, June 2008.

- [3] *Measuring Power and Temperature from Real Processors*, Francisco-Javier Mesa-Martinez, Michael Brown, Joseph Nayfach-Battilana, Jose Renau, The Next Generation Software (NGS) Workshop (NGS08) held in conjunction with IPDPS, April 2008.
- [4] *uDSim, a Microprocessor Design Time Simulation Infrastructure*, Sangeetha Sudhakrishnan, Francisco-Javier Mesa-Martinez, Jose Renau, Wild and Crazy Ideas VI (WACI) held in conjunction with ASPLOS, March 2008.
- [5] *Printed Circuit Board Layout Time Estimation*, Cyrus Bazeghi and Jose Renau, 7th Workshop on Complexity-Effective Design (WCED), held in conjunction with ISCA-33, June 2006.
- [6] *SCOORE: Santa Cruz Out-of-Order RISC Engine, FPGA Design Issues*, Francisco J. Mesa-Martinez, Abhishek Sharma, Andrew W. Hill, Carlos A. Cabrera, Cyrus Bazeghi, Hari Kolakaleti, Joseph Nayfach, Keertika Singh, Kevin S. Halle, Matthew D. Fischler, Melisa Nunez, Sangeetha Nair, Suraj Narender Kurapati, Wael Ali Ashmawi, and Jose Renau, Workshop on Architectural Research Prototyping (WARP), held in conjunction with ISCA-33, June 2006.
- [7] *Profile-Based Energy Reduction for High Performance*, Wei Huang, Jose Renau, and Josep Torrellas, ACM Workshop on Feedback-Directed and Dynamic Optimization (FDDO), December 2001.
- [8] *Energy/Performance Design of Memory Hierarchies for Processor-In-Memory Chips*, Wei Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, Workshop on Intelligent Memory Systems, November 2000. It also appeared in Lecture Notes in Computer Science (Vol. 2107) by Springer-Verlag, 2001.
- [9] *Memory Hierarchies in Intelligent Memories: Energy/Performance Design*, Wei Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, Ninth Workshop on Scalable Shared Memory Multiprocessors, June 2000.

Synergistic Collaborations/Technology Transfer

- Sun Microsystems is using the UCSC thermal setup to thermally validate their future processors (Rock)
- Collaborate with NVIDIA to measure GPU thermal characteristics. Measurements are used by product division
- Director of the OpenSPARC Sun Center of Excellence at UCSC
- Founding member of OpenSPARC community governance board
- Maintain SESC (<http://sesc.sourceforge.net>). SESC is an architectural simulator used by several universities.
- Maintain XCACTI. An extension of CACTI with several improvements used by several universities.

Talks

As Presenter at Conferences/Workshops/Panel

- *DSim, a Microprocessor Design Time Simulation Infrastructure*, WACI (held with ASPLOS), March, 2008.
- *Complexity Panel at WCED 2006*, WCED (held with ISCA), June 2006.
- *SESC, a Chip Multiprocessor Simulator*, Multicore Expo, April 2006.
- *Thread-Level Speculation on a CMP Can Be Energy Efficient*, International Conference on Supercomputing (ICS), June 2005.
- *Cherry: Checkpointed Early Resource Recycling in Out-of-order Microprocessors*, International Symposium on Microarchitecture (MICRO), November 2002.

- *Cache Decomposition for Energy-Efficient Processors*, International Symposium on Low Power Electronics and Design (ISLPED), August 2001.
- *Memory Hierarchies in Intelligent Memories: Energy/Performance Design*, The Ninth Workshop on Scalable Shared Memory Multiprocessors, June 2000.

As Invited Speaker

- *Power and Thermal Research at UCSC*, DCGSystems, August 2009.
- *SPEC Thermal Characterization*, RAMP Retreat June 2009.
- *Thermal Research at the MASC Group*, AMD, April 2009.
- *Thermal Research at UCSC*, NVIDIA, March 2009.
- *Power and Thermal Models for RAMP2*, RAMP Retreat January 2009.
- *Micro Architecture at Santa Cruz*, University of Illinois Urbana-Champaign, February 2008.
- *Micro Architecture at Santa Cruz*, UC Berkeley, February 2008.
- *Processor Verification with hwBugHunt*, RAMP Retreat January 2008.
- *Thread Level Speculation and Thermal Modeling*, NVIDIA, November 2007.
- *OpenSPARC Center of Excellence Announcement*, Worldwide Education and Research Conference, San Francisco, February 2007.
- *Micro Architecture at Santa Cruz*, Cornell University, February 2007.
- *Thermal Modeling and Processor Pruning*, Stanford University, January 2007.
- *Thermal Modeling*, SUN Microsystems, Santa Clara, December 2006.
- *Micro Architecture at Santa Cruz*, Altera, San Jose, February 2006.
- *Micro Architecture at Santa Cruz*, Intel Research Lab, Santa Clara, January 2006.
- *Micro Architecture at Santa Cruz*, SUN Microsystems, Santa Clara, November 2005.
- *Design Complexity Metrics*, Numetrics, Cupertino, August 2005.
- *Design Complexity Metrics*, Intel Research Lab, Santa Clara, August 2005.
- *Chip Multiprocessors with Thread Level Speculation*, Intel Research Lab, Santa Clara, December 2004.
- *Architectural Support for Hierarchical Thread-Level Speculation*, IBM T.J.Watson Research Center, New York, August 2003.

Infrastructure Developed

- Designed and implemented a new simulator of computer architectures (SESC). It is used by several research groups at the University of Illinois, University of Rochester, North Carolina State University, Georgia Institute of Technology, and Cornell University. It models a variety of architectures, including dynamic superscalar processors, CMPs, processor-in-memory, and TLS architectures.
- Created a fully automatic TLS compiler pass using GCC. It generates tasks with software value prediction. This is the compiler used to evaluate the architecture proposed in my Ph.D. thesis.
- Extend CACTI's energy model. CACTI is a widely used cache power model. The extensions have been used at the University of Illinois, University of Rochester, North Carolina State University, U.C. Davis, U.C. Irvine, U.C. Riverside, and University of Arizona.
- Contributed to official Shared Memory Multiprocessors (SMP) Linux patches to support SMP boards. These patches are included in all the Linux kernel distributions since 1995.
- Co-developed the IEEE 1284 (parallel port) in Linux. This implementation is included in all Linux kernels since 1996.
- Developed official GCC patches, which are included in the main distribution (2002).

- Developed TCP/IP over SCSI boards, which involved several modifications to the Linux kernel to support a high-performance interconnection system between Linux machines.
- Invented a new data compression algorithm (ILZR), a variant of Lempel Zib Ross William, distributed as public domain for Amiga Computers in Aminet-CD (1993).
- Developed the superscalar simulation infrastructure used by the Architecture Group at the Computer Science Department of Ramon Llull University (1992-1994).

Teaching

- cmpe202, Computer Architecture
- cmpe221, Advanced Microprocessor Design
- cmpe126, Advanced Logic Design
- cmpe110, Computer Architecture

Professional Experience

Jul 2004- Assistant Professor. University of California, Santa Cruz.

Jan 1999-Jun 2003 Research Assistant. University of Illinois at Urbana-Champaign.

Aug 1998-Dec 1998 System Administrator. University of Illinois at Urbana-Champaign.
Worked for the Computing and Communications Services Office.

Jan 1998-Jul 1998 Computer Network Specialist. FIHOCA, S.A. (Spain).

Sep 1996-Sep 1997 System Administrator. Asertel, S.A. (Spain).

In charge of the computer infrastructure. Specialized in network security.

May 1995-Sep 1996 Systems Manager. Ramon Llull University (Spain).

In charge of the administration of the UNIX machines, PCs, and the network of the University.

Professional Activities and Memberships

- Program Committee service: MICRO 09, ICPP 09, HotChips 09, ICCD 09, ICCD 08, HotChips 08, ICCD 07, IPDPS 07, ICCD 06
- Other Committee service: PACT 05 web chair, SC 07 publicity chair.
- Reviewer of papers for conferences and journals in computer architecture (ISCA, MICRO, HPCA, ICS, ICPP, CAL, ICCD, and IPDPS).
- Peer Reviewer for NSF proposals

UCSC Visitors Hosted

- 2009:
 - Jose Luis Briz, University of Zaragoza, Spain
 - Jose Ignacio Martinez Torre, Universidad Rey Juan Carlos, Spain
 - Gary Tyson, Florida State University
 - Sai Ankireddi, Sun Microsystems
- 2008:
 - Krste Asanovic, Berkeley University
 - Don Le, John Nickolls, and Massimiliana Fatica, NVIDIA
 - Shrenik Mehta, Denis Sheahan, Sun Microsystems
 - Derek Chiou, University of Texas
 - Jose Luis Briz, University of Zaragoza, Spain
 - Vishak Venkatraman, AMD
- 2007:
 - Luigi Capodiecici, AMD
 - Michael Gschwind, IBM T.J. Watson
 - Christos Kozyrakis, Stanford University
- 2006:
 - David Weaver and Grace Caulfield, Sun Microsystems
 - Miguel Ullan, Centro Nacional de Microelectronica (Spain)
 - Albert Cohen and Sebastian Pop, INRIA (France)
 - Matt Hancher, NASA
 - Ayal Zaks, IBM (Isreal)
- 2005:
 - Konstantin Lukin, Scientific and Technology Center (Ukraine)