

CURRICULUM VITAE

October 25, 2009

Matthew R. Guthaus

Baskin School of Engineering, E2-225
University of California Santa Cruz
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EMPLOYMENT

University of California Santa Cruz, Santa Cruz, CA USA

Assistant Professor, July 2006 –

Current research focuses on reliability and variability of Integrated Circuits (ICs). Specific projects mostly deal with thermal-aware design of clock trees, floorplans, and mixed-signal systems. In addition, algorithm-specific computation is a primary research area and is used as a test design for the prior projects.

University of Michigan, Ann Arbor, MI USA

Graduate Student Research Assistant, Aug. 1998 – April 2003, April 2005 – Sept. 2006

Researched the impact of manufacturing variation due to front-end and back-end sources on circuit performance. Designed and implemented automated design techniques to improve parametric yield through circuit sizing and clock tree construction. Previous projects include the specification, design and testing of several mixed-signal microcontrollers (MS8 and WIMS) and physical cell design for a high-speed GaAs microprocessor (PUMA).

IBM T.J. Watson Research Center, Yorktown Heights, NY USA

Supplemental Researcher, April 2003 – April 2005

Performed research on various aspects of physical design including: gate sizing, detailed routing congestion analysis, buffering, and physical synthesis using statistical timing.

National Semiconductor Corporation, San Jose, CA USA

ASIC Consultant, May 1999 – May 2000

Wrote the specification and RTL implementation of a COP8-compatible microcontroller that included flash memory, multifunction timers, and other peripherals.

University of Michigan, Ann Arbor, MI USA

Graduate Student Instructor, Aug. – Dec. 1999, Jan. – May 2001

Created a standard cell, hierarchical design flow based on Cadence's Silicon Ensemble and Synopsys' Design Compiler for the Advanced VLSI Design course. Led a weekly discussion section that introduced the ASIC design flow, design automation, and helped with individual group challenges.

International Business Machines, Rochester, MN USA

AS/400 Processor Design Co-op, May 1997 – Dec. 1997

Assisted Fixed Point and Instruction Unit teams in multiple phases of PowerPC processor development. Developed a multi-processor randomized memory coherence verification tool and worked on the design and simulation of a semicustom macro (L1 by-pass mux).

Computer-Aided Engineering Network, Ann Arbor, MI USA

Unix Support/Webmaster, June 1996 – May 1997

Responsibilities included answering user questions, server administration and writing Perl CGI scripts.

EDUCATION

University of Michigan, Ann Arbor, MI USA

Ph.D. Electrical Engineering, 2006.

Thesis:

“Clock Tree Analysis and Synthesis Considering Process Parameters and Variability”

M.S.E. Electrical Engineering, 2000.

Emphasis: VLSI and CAD

B.S.E. Computer Engineering, 1998.

Emphasis: Computer architecture, software, and VLSI

Western Michigan University, Kalamazoo, MI USA

Select Mathematics & Computer Science Courses during High School, 1993-1994.

Kalamazoo Area Mathematics and Science Center, Kalamazoo, MI USA

Intensive Mathematics & Science Magnet High School, 1994.

PROFESSIONAL COMPETENCE AND ACTIVITY

Honors and Awards

- A1 Eta Kappa Nu Most Outstanding Active Member, 1997.
- A2 University of Michigan, Magna Cum Laude, 1998.
- A3 James B. Angell Scholar, 1999.
- A4 M.R. Guthaus and K.L. Kraver. “A Low-Power, Mixed-Signal Microcontroller for Single Chip Instrument Applications,” DAC 2000 Student Design Contest Honorable Mention, 38th Design Automation Conference, 2000.
- A5 GAANN Fellowship, 2000.
- A6 Mobius Integrated Systems (M. McCorquodale, M.R. Guthaus, and K. Kraver). Finalist, UMBS’s Pryor-Hale Business Plan Competition, 2001.
- A7 Mobius Integrated Systems (M. McCorquodale, M.R. Guthaus, and K. Kraver). Finalist, Innovators Business Pitch Competition, 2001.
- A8 M.R. Guthaus and D. Motter. First Place, First Annual ACM/SIGDA CADAthlon programming competition. San Jose, CA, 2002.

- A9 R.M. Senger, E.D. Marsman, M.S. McCorquodale, F.H. Gebara, K.L. Kraver, M.R. Guthaus, R.B. Brown. "A 16-Bit Mixed-Signal Microsystem with Integrated CMOS-MEMS Clock Reference," The Joint Design Automation Conference and International Solid State Circuits Conference Student Design Competition: First Place, Conceptual Category, Anaheim, 2003.
- A10 M.R. Guthaus and J. Roy. First Place, Fourth Annual ACM/SIGDA CADAthlon programming competition. San Jose, CA, 2005.
- A11 Fellow of Crown College, September 2008.
- A12 ACM SIGDA Service Award, July 2009.

Grants

- G1 PI, DE-2 Educational Development FPGA Boards, Altera University Program, \$2,475, October 2006.
- G2 Co-PI (PI: Jose Renau), Sun Center of Excellence equipment donation, \$120,000, February 2007.
- G3 PI, Faculty Improvement Award, UCSC, \$2,500, 2007-2008.
- G4 PI, Multi-Project IC for Variability, Reliability and Skew Tolerant Clocking, COR Special Research Grant, \$20,000, 2006-2007.
- G5 PI, Faculty Improvement Award, UCSC, \$2,000, 2008-2009.
- G6 Co-PI, (PI: Jose Renau, Co-PIs: Ali Shakouri, Sung-Mo "Steve" Kang) SMA: Accurate Temperature Measurement Infrastructure and Methodology for Power, Variability, and Reliability Analysis, NSF Computer Systems Research, \$300,000, January 2007.
- G7 PI, Xilinx Software and Equipment Development FPGA Boards, Xilinx University Program, \$1,506, October 2008.
- G8 PI, Faculty Improvement Award, UCSC, \$1,000, 2009-2010.
- G9 PI, Revising Advanced Logic Design to Include Hardware/Software Co-design, UCSC, Course Development Fellowship, \$9,325, 2010-2011.
- G10 PI, Radiation Hard Field-Programmable Gate Array (FPGA) Synthesis, NASA UARC, \$43,000, 2009-2010.
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PUBLICATIONS

The author list is indicated exactly as it appears on each paper.

Legend:

- [G] indicates my graduate student or postdoc is listed as first author; this is my policy,
- [A] indicates I did all of the work for this paper,
- [M] indicates I did most of the work for this paper,

- [*S*] indicates I did a significant amount of the work on this paper,
- [*T*] indicates work was related to my M.S. or Ph.D. thesis,
- [*P*] indicates the paper was a peer-reviewed publication.

Journals

- J1 [*S, P*] K.L. Kraver, M.R. Guthaus, T.D. Strong, P.L. Bird, G.S. Cha, W. Hold, R.B. Brown. "A mixed-signal sensor interface microinstrument," *Sensors and Actuators A*, vol. 91, pp. 266-277, 2001.
- J2 [*S, P*] R.A. Ravindran, R.M. Senger, E.D. Marsman, G.S. Dasika, M.R. Guthaus, S.A. Mahlke, R.B. Brown. "Partitioning variables across register windows to reduce spill code in a low-power processor," *IEEE Transactions on Computers*, Volume 54, Issue 8, August 2005, pp 998-1012.

Conferences, Workshops, and Symposia

- C1 [*S, P*] K.L. Kraver, M. R. Guthaus, T.D. Strong, P.L. Bird, G.S. Cha, W. Hoeld, and R.B. Brown. "A Mixed-Signal Sensor Interface Microinstrument," *Hilton Head Solid State Sensors and Actuators Workshop*, 2000.
- C2 [*A, P*] M.R. Guthaus, J.S. Ringenberg, D. Ernst, T.M. Austin, T. Mudge, R.B. Brown. "MiBench: A Free, Commercially Representative Embedded Benchmark Suite," *IEEE 4th Annual Workshop on Workload Characterization*, 2001. (831 citations as of 06/26/09)
- C3 [*S, P*] R. Berger, E. Chan, D. Rickard, B. Clegg, S. Patton, R. Anderson, R. Brown, D. Sylvester, M. Guthaus, H. Deogun, J.R. Liu, C. Pandana, and N. Chandrachoodan. "BAE Systems Mission Specific Processor Technology," *GOMAC*, Tampa, FL, 2003.
- C4 [*S, P*] S.M. Martin, R.M. Senger, E.D. Marsman, F.H. Gebara, M.S. McCorquodale, K.L. Kraver, M.R. Guthaus, and R.B. Brown, "A Low-Power Microinstrument for Chemical Analysis of Remote Environments," *11th NASA Symp. on VLSI Design*, Coeur d' Alene, ID, May 28-29, 2003, pp 1-4.
- C5 [*S, P*] R.A. Ravindran, R.M. Senger, E.D. Marsman, G.S. Dasika, M.R. Guthaus, S.A. Mahlke, and R.B. Brown, "Increasing the Number of Effective Registers in a Low-Power Embedded Processor Using a Windowed Register File," *International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)*, San Jose, CA, October 31 - November 1, 2003. (acceptance rate $31/162=19\%$)
- C6 [*S, P*] M.S. McCorquodale, E.D. Marsman, R.M. Senger, F.H. Gebara, M.R. Guthaus, D.J. Burke, and R.B. Brown, "Microsystem and SoC Design with UMIPS," *IFIP VLSI System-on-a-Chip Conference (VLSI-SOC)*, Darmstadt, Germany, December 1-3, 2003, 324-329.
- C7 [*M*] M. Guthaus, D. Kung, J. Narasimhan, R. Puri, L. Trevillyan, and C. Visweswariah. Variability-aware design optimizations using statistical timing. *IBM Academy Conference on Design for Manufacturability*, Somers, NY, May, 2004.
- C8 [*S, P*] E.D. Marsman, R.M. Senger, M.S. McCorquodale, M.R. Guthaus, R.A. Ravindran, G.S. Dasika, S.A. Mahlke, and R.B. Brown. "A 16-Bit Low-Power Microcontroller with

Monolithic MEMS-LC Clocking,” International Symposium on Circuits and Systems (IS-CAS), Kobe, Japan, May 23-26, 2005.

- C9 [A, P] M.R. Guthaus, N. Venkateswaran, D. Sylvester, R.B. Brown, and V. Zolotov. “Optimization Objectives and Variation Models for Statistical Gate Sizing,” Great Lakes Symposium on VLSI (GLSVLSI), Chicago, IL, April 17-19, 2005, pp. 312-316. (acceptance rate $52/239=21.76\%$ for full papers)
- C10 [A, P] M.R. Guthaus, N. Venkateswaran, C. Visweswariah, V. Zolotov. “Gate Sizing using Incremental Parameterized Statistical Timing Analysis,” International Workshop on Logic Synthesis (IWLS), Lake Arrowhead, CA, June 8-11, 2005.
- C11 [A, P] M.R. Guthaus, N. Venkateswaran, C. Visweswariah, V. Zolotov. “Gate Sizing using Incremental Parameterized Statistical Timing Analysis,” International Conference on Computer-Aided Design (ICCAD), San Jose, CA, November 7-10, 2005, pp. 1029-1036. (acceptance rate $128/480=23.7\%$)
- C12 [A, T, P] M.R. Guthaus, D. Sylvester, R.B. Brown. “Process-Induced Skew Reduction in Nominal Zero-Skew Clock Trees,” Asia-South Pacific Design Automation Conference (ASPDAC), Yokohama, Japan, January 24-27, 2006, pp. 84-89. (acceptance rate $135/432=31.25\%$)
- C13 [A, T, P] M.R. Guthaus, D. Sylvester, R.B. Brown. “Clock Buffer and Wire Sizing using Sequential Quadratic Programming,” Design Automation Conference (DAC), San Francisco, CA, July 24-28, 2006, pp. 1041-1046. (acceptance rate $160/865=18.5\%$)
- C14 [A, T, P] M.R. Guthaus, D. Sylvester, R.B. Brown. “Clock Tree Synthesis with Data-path Sensitivity matching,” Asia-South Pacific Design Automation Conference (ASPDAC), Seoul, Korea, January 21-24, 2008, pp. 498-503. (acceptance rate $122/350=35\%$)
- C15 [A, P] M.R. Guthaus. “Teaching VLSI Design in 10 Weeks,” Microelectronic Systems Education Conference (MSE), San Francisco, CA, 2009, pp. 41-44.
- C16 [S, P] M. Brown, C. Bazeghi, M.R. Guthaus, J. Renau, “Measuring and Modeling Variability using Low-Cost FPGAs”, Workshop on Modeling, Benchmarking, and Simulation (MoBS), Austin, TX, 2009.
- C17 [G, M, P] K. Woo, M.R. Guthaus. “Fault Tolerant Synthesis using Non-Uniform Redundancy,” International Workshop on Logic Synthesis (IWLS), Berkeley, CA, 2009.
- C18 [G, M, P] S. Logan, M.R. Guthaus. “Thermal-Aware Floorplanning using Whitespace Allocation,” IFIP VLSI System-on-a-Chip Conference (VLSI-SOC), Florianopolis, Brazil, 2009, IN PRESS.
- C19 [G, M, P] K. Woo, M.R. Guthaus. “Fault Tolerant Synthesis using Non-Uniform Redundancy,” International Conference on Computer Design (ICCD), Lake Tahoe, CA, 2009, IN PRESS.

Invited Papers

- I1 [S, P] R.M. Senger, E.D. Marsman, M.S. McCorquodale, F.H. Gebara, K.L. Kraver, M.R. Guthaus, R.B. Brown. “A 16-Bit Mixed-Signal Microsystem with Integrated CMOS-MEMS Clock Reference,” Design Automation Conference (DAC) Invited Paper, June 2003, pp. 520-525.

Submitted Works and Works in Progress

Scholarly Talks

- T1 “Approaches to Low-Power Microcontroller Design,” WIMS ERC Industrial Advisory Board Meeting, Ann Arbor, MI, October, 2001.
- T2 “MiBench: A Free, Commercially Representative Embedded Benchmark Suite,” IEEE 4th Annual Workshop on Workload Characterization, Austin, TX, December 2001.
- T3 “Automated Semicustom Design using Standard Cell Synthesis,” Delphi Automotive, January, 2002.
- T4 “Optimization Objectives and Variation Models for Statistical Gate Sizing,” Great Lakes Symposium on VLSI (GLSVLSI), Chicago, IL, April 17-19, 2005.
- T5 “Gate Sizing using Incremental Parameterized Statistical Timing Analysis,” International Workshop on Logic Synthesis (IWLS), Lake Arrowhead, CA, June 8-11, 2005.
- T6 “Gate Sizing using Incremental Parameterized Statistical Timing Analysis,” International Conference on Computer-Aided Design (ICCAD), San Jose, CA, November 7-10, 2005.
- T7 “Process-Induced Skew Reduction in Nominal Zero-Skew Clock Trees,” Asia-South Pacific Design Automation Conference (ASPDAC), Yokohama, Japan, January 24-27, 2006.
- T8 “VLSI Design of Embedded Systems-on-Chips”, Cornell University, Ithaca, NY, February 2, 2006.
- T9 “Clock Tree Analysis and Synthesis Considering Process Variation”, University of California Santa Cruz, Santa Cruz, CA, February 16, 2006.
- T10 “Clock Tree Analysis and Synthesis Considering Process Variation”, Brown University, Providence, RI, February, 2006.
- T11 “Clock Buffer and Wire Sizing using Sequential Quadratic Programming,” Design Automation Conference (DAC), San Francisco, CA, July 24-28, 2006.
- T12 “Clock Tree Synthesis with Data-path Sensitivity matching,” Asia-South Pacific Design Automation Conference (ASPDAC), Seoul, Korea, January 21-24, 2008.
- T13 “Thermal Research at UCSC”, NVIDIA Corporation, Santa Clara, CA, March, 2009.
- T14 “A Dynamic Programming Algorithm for Area-Efficient Fault Tolerant Circuits,” Ambient GCOE VLSI Workshop, Waseda University, Tokyo, Japan, September 8, 2009.
- T15 “Electronic Design Automation for Reliable Microelectronics”, University of Utah, Salt Lake City, UT, September 21, 2009.

Posters

- P1 [A, P] M.R. Guthaus and K.L. Kraver. “A Low-Power, Mixed-Signal Microcontroller for Single Chip Instrument Applications,” SIGDA University Booth, 2000.
- P2 [A, T, P] M.R. Guthaus, “Robust Design using Parametric Statistical Optimization”, Poster, Design Automation Conference (DAC) PhD Forum, Anaheim, CA, 2005.

- P3 [*S, P*] M. Brown, C. Bazeghi, M.R. Guthaus, J. Renau, "Measuring and Modeling Variability using Low-Cost FPGAs", FPGA Symposium, Monterey, CA, 2009.
- P4 [*A, P*] M.R. Guthaus. "Teaching VLSI Design in 10 Weeks," Microelectronic Systems Education Conference (MSE), San Francisco, CA, 2009.
- P5 [*G, M, P*] S. Logan and M.R. Guthaus, "Fast Thermal-Aware Floorplanning", SIGDA University Booth, San Francisco, CA, 2009.
- P6 [*A, P*] M.R. Guthaus. "Teaching VLSI Design in 10 Weeks," SIGDA University Booth, San Francisco, CA, 2009.
- P7 [*G, M, P*] X. Hu and M.R. Guthaus, "Thermal-Aware Clock Tree Synthesis", 5th Annual UCSC Graduate Research Symposium, 2009.
- P8 [*G, M, P*] K. Woo and M.R. Guthaus, "Fault-Tolerant Synthesis using Non-Uniform Redundancy", 5th Annual UCSC Graduate Research Symposium, 2009.
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UNIVERSITY SERVICE

Department

Computing Infrastructure Committee (CIC) Member, February 2007-current.

School of Engineering

Synopsys/UCSC Primary Technical Support Contact, 2006-current.

Cadence/UCSC Technical Support Contact, 2006-current.

IEEE Student Chapter, Advisor, 2009-current.

Hardware Projects Lab, Advisor, 2009-current.

Other

Engineering Advisory Board for UCSC Extension, 2008-current.

OUTSIDE PROFESSIONAL ACTIVITIES

Professional Service

SIGDA/ACM CADathlon Programming Contest, Co-Chair, 2006

SIGDA/ACM CADathlon Programming Contest, General Chair, 2007.

SIGDA/ACM CADathlon Programming Contest, SIGDA Liason, 2008.

SIGDA/ACM CADathlon Programming Contest, General Chair, 2009.

ACM/SIGDA Advisory Board, 2008-current.

IEEE Monterey Bay, Vice-Chair, 2008-current.

Memberships

IFIP Working Group 10.5 Design and Engineering of Electronic Systems, Member, 2009 –

CANDE (Computer-Aided Network DEsign) Committee, Member, 2007 –

Association for Computing Machinery, SIGDA Member, 2006 –

Institute of Electrical & Electronics Engineers, Member, 2006 –

Association for Computing Machinery, SIGDA Student Member, 2000 – 2006

Institute of Electrical & Electronics Engineers, Student Member, 1995 – 2006.

Eta Kappa Nu (HKN) Honor Society, Member, 1996–

Eta Kappa Nu (HKN) Honor Society, Committee Chairperson, 1996–1998.

Member of Student Projects Lab Founding Group, 1998.

Michigan Student Society of Professional Engineers, Correspondence Secretary, 1994–1996.

Conference Participation

DAC Session Chair Session 40: Performance Driven Layout Optimization, 2008.

DAC Session Chair Session 9: Statistical Methods in Static Timing Analysis, 2009.

VLSI-SOC Session Chair Session M3A: 3D Integration, 2009.

ICCAD Session Chair Session 5B: Congestion Driven Placement, 2009.

VLSI-SOC Special Session Organizer, 2010.

Conference Service

IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) Publicity Chair, 2007.

IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) Technical Program Committee, 2007.

IEEE Electronic Design Processes (EDP) Advisory Board, 2008.

IFIP Educational Technology (EduTech) Technical Program Committee, 2009.

IEEE Electronic Design Processes (EDP) Advisory Board, 2009.

IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI) Technical Program Committee, 2009.

IEEE/ACM Asia-South Pacific Design Automation Conference (ASP-DAC) Technical Program Committee, 2009.

IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) Technical Program Committee, 2009.

IEEE/ACM Asia-South Pacific Design Automation Conference (ASP-DAC) Technical Program Committee, 2010.

IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) Technical Program Committee, 2010.

IEEE Latin American Symposium on Circuits and Systems (LASCAS) Technical Program Committee, 2010.

IEEE International Conference on Microelectronic Systems Education (MSE) Poster Chair, 2011.

IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) General Chair, 2012.

Editorial Service

SIGDA E-Newsletter Editor, 2006-current.

Journal, Conference and Book Reviews

IEEE Transactions on VLSI Systems, 2000-current

IEEE/ACM Design Automation Conference, 2002-current

International Conference on Computer-Aided Design, 2002-current

Closing the Gap Between ASIC & Custom Tools and Techniques for High-Performance ASIC Design by David Chinnery and Kurt Keutzer, Kluwer Academic Publishers, ISBN 1-4020-7113-2, May 2002, 432 pp.

International Symposium on Physical Design (ISPD), 2003

Integration, the VLSI Journal, 2005-current

Timing Analysis and Uncertainty Workshop (TAU), 2006

IEEE Transactions on Computer-Aided Design, 2007-current

IEEE Transactions on Computers, 2008-current

IEEE/ACM Asia-South Pacific Design Automation Conference (ASP-DAC), 2008-current

ACM Journal of Educational Resources in Computing, 2009-current

IEEE/ACM Great Lakes Symposium on VLSI, 2009-current

OTHER

Significant Projects

Clock Optimization using Parametric Statistical Static Timing Analysis

Researched algorithms to decrease the susceptibility of clock trees to manufacturing variation. Implemented a C++ clock tree statistical analysis tool that included interconnect

and device variations. The analysis framework was used to investigate extensions of the Deferred Merge Embedding (DME) trees for reduced statistical skew. The analysis was also used in the implementation of a sequential quadratic programming (SQP) approach to buffer and wire sizing.

Gate-Sizing using Parametric Statistical Static Timing Analysis

Performed the initial integration of EinsStat, the IBM statistical static timing analyzer, and PDS, the IBM placement driven synthesis tool. Subsequently developed a sensitivity-based gate sizing algorithm using the statistical criticality metrics as guidance.

Simulated Annealing Standard Cell Placement

Implemented an extension to the Capo fixed-die placer to perform optimization using simulated annealing. The additional classes used the UCLA database source code as the foundation and added methods for random cell permutation and temperature scheduling.
<http://vlsicad.eecs.umich.edu/BK/PDtools/>

Wireless Integrated Microsystems (WIMS) Microcontroller

Specified the instruction set architecture (ISA) and initial system specification of a 16-bit microcontroller intended for use in environmental sensor devices and cochlear implants. Wrote the assembler and guided beginning graduate students in the initial phases of the project.

<http://www.wimserc.org>

Gain-based Static Timing Analysis and Gate Sizing

Designed a static timing framework that used analytic, gain-based timing models. The static timing framework was used in the implementation of several sizing algorithms including a TILOS-like algorithm and a logical effort algorithm. This project was part of the DARPA Complex Signal Processing ASIC Designs grant that is oriented at improving the performance of ASIC methodologies for signal processing designs.

Mixed-Signal 8-bit Microcontroller

Specified, implemented, and tested an 8-bit microcontroller with an assortment of peripherals including USART, multifunction timers, multiply-accumulate unit, and software controlled power management. This project was used as the basis of the proposal for the microelectronics thrust of a \$22M, 10 year ERC in Wireless Integrated Microsystems at the University of Michigan.

<http://www.eecs.umich.edu/ms8>

Research Community Contributions

UMIPS: University of Michigan Intellectual Property Source

UMIPS was founded in 2003 and is a collaborative effort between Electrical Engineering and Computer Science students, faculty, and researchers to leverage each others' integrated circuit development in the pursuit of cutting-edge circuits and microsystems research. The idea behind UMIPS is design reuse and its importance to research. There is no reason why researchers should burn time and resources developing either trivial blocks that could be reused or blocks that do not add significant value to their research. This "reinventing the wheel" syndrome of integrated circuit design is exactly the problem that UMIPS identified and set out to remedy.

<http://www.eecs.umich.edu/umips>

MiBench: A free, commercially representative embedded benchmark suite

Academic researchers have had a problem with realistic, embedded benchmarks like the Embedded Microprocessor Benchmarking Consortium (EEMBC, <http://www.eembc.org>). The EEMBC benchmarks are not available to academic users. MiBench is a set of freely available source codes in the following categories: automotive and industrial control, networking, security, consumer devices, telecommunications, and office automation. The benchmarks are currently used by several research groups and major corporations including IBM, ARM and Motorola.

<http://www.eecs.umich.edu/mibench>

Languages

English (native)

Japanese (intermediate, 2 years at college level)

Spanish (beginner)

CAD Tools

IBM (PDS, EinsTimer, EinsStat)

Mentor Graphics (IC Station)

Cadence (Silicon Ensemble, Virtuoso)

Synopsys (Design Compiler, PrimeTime, PathMill, AMPS)

Prolific (Prospin, Progen)

Programming Languages

Python

C/C++

Perl

Bash

Verilog

Assembly (PowerPC, MIPS, COP8)

Other

General systems administration knowledge.

Have used GNU/Linux since 1994.

TEACHING**Courses Taught (None co-taught)**

Term F/W/S	Course	Description	Enrolled	% Evals Returned	Instructor Overall %	Course Overall %
S2009	CMPE 100/L	Intro. to Logic Design	42	88.0	88.4	87.0
W2009	CMPE 100/L	Intro. to Logic Design	19	89.5	90.0	88.8
W2009	CMPE 280G	Seminar in VLSI				
F2008	CMPE 222	VLSI Dig. Sys. Design	9	100	85.8	88.8
F2008	CMPE 280G	Seminar in VLSI	6	83.3	96.0	96.0
S2008	CMPE 126/L	Adv. Logic Design	7	85.7	86.6	84.0
S2008	CMPE 280G	Seminar in VLSI				
W2008	CMPE 223	VLSI SoC Design	9	77.8	85.8	77.4
W2008	CMPE 280G	Seminar in VLSI				
F2007	CMPE 222	VLSI Dig. Sys. Design	9	88.9	88.4	93.4
S2007	CMPE 125/L	Log. Design w. Verilog	6	100.0	91.6	90.0
F2006	CMPE 222	VLSI Dig. Sys. Design	9	88.9	94.2	93.4
*W2001	EECS 627	VLSI Design II (TA)	-	-	94.2	-
*F1999	EECS 627	VLSI Design II (TA)	-	-	98.0	-

* indicates at The University of Michigan

Courses Modified and/or Created

Revised CMPE 125/L and CMPE 126/L courses and prerequisites, Fall 2006.

Revised CMPE 222 course outline and prerequisites, Fall 2006.

Created CMPE 280G seminar on VLSI, Winter 2008

Created new course CMPE 223, VLSI System-on-a-Chip Design, Winter 2008.

Revising Advanced Logic Design to Include Hardware/Software Co-design, UCSC, Course Development Fellowship, 2010-2011.

Students

Name	Start	Grad.	Thesis
PhD Alumni			
PhD Candidates			
Logan, Sheldon	W2007		
PhD Students			
Condley, Walter	F2009		
Hill, Andrew	F2009		
hline Hu, Xuchu	F2008		
Jamil, Mohammed	F2007		
Kim, Seokjoong	F2008		
Sankaranarayanan, Rajsaktish	F2009		
Siero, Marcelo	F2009		
Woo, Keven	F2007		
MS Alumni			
Das, Suparna	F2006	S2008	Adaptive Clocking and Dynamic Error Detection in ICs
MS Students			
Chan, Derek	W2006		
Srivatsaa, Vidyuth	F2009		
Natesh, Pranav	F2009		
Undergraduate Alumni			
Condley, Walter	W2008	S2009	-
Undergraduate Students			
Peters, Chase	F2009		-

Other Thesis Committees

Name	Advisor	Degree	Year	Thesis
Golubev, Tom	Renau	BS	2009	The ATC - Automatic Testbench Creator
Munday, David	Renau	MS	2009	L0 Speculative Data Cache for High Performance Out-of-Order Superscalar Processors
Bazhegi, Cyrus	Renau	PhD	2007	System and Processor Design Effort Estimation: Using Complexity and Variability to Explore New Opportunities for Optimization
Poonawala, Aryn	Milanfar	PhD	2007	Mask Design for Single and Double Exposure Optical Microlithography: An Inverse Imaging Approach
Mesa-Martinez, Francisco	Renau	PhD	2007	Exploiting Design Complexity to Expose New Opportunities for Processor Optimization
Wu, Huaizhi	Schlag	PhD	2007	A Low Power Design Methodology with Multi-Vdd and Voltage Islands
Li, Wei	Kang	PhD	2007	Thermal-aware placement methodology
Hoang, Linh	Liu	MS	2007	Digital Architecture for High Resolution Micro-Stimulation for Retinal
Kurapati, Suraj	Renau	MS	2007	Specification-driven functional verification with Verilog PLI & VPI and SystemVerilog DPI
Schmidt, Angela	Renau	MS	2007	Hardware Predictors on SESC