7

Nanoelectronics Applications

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Carbon nanotubes are either semiconducting or metallic depending on their structures [1–5] as discussed in Chapter 1. Usually, semiconductors are used for metal-semiconductor (Schottky) diodes, pn junction diodes, and field-effect transistors (FETs), whereas metals are used for single-electron tunneling transistors. This situation is more or less the same in nanotube (NT) electronics. In this chapter, semiconducting NT devices will be emphasized. Semiconducting NT characterization is discussed in Section 7.1, followed by doping in Section 7.2, NT FETs in Section 7.3, intermolecular NT Schottky junctions in Section 7.4, and NT pn junctions as Esaki diodes in Section 7.5. Coulomb blockade phenomena are observed in both semiconducting and metallic NTs. Coulomb oscillations and Coulomb diamonds are covered in Section 7.6. In Section 7.7, other semiconducting NT devices are examined, and some topics in metallic NT transport are briefly covered in Section 7.8. Finally, in Section 7.9, general remarks on nanoFETs, including NT FETs, are given.

7.1 Carrier Characterization

In electronics applications, semiconductors must be identified as p-type or n-type. In the NT field, the thermoelectric power measurement and the FET are used for this purpose.

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7.1.1 Thermoelectric Power Measurement

In the thermoelectric power measurement [6], the doping nature is determined by the sign of Seebeck voltage generated by a temperature gradient [7] with a hot probe and a cold probe as shown in Figure 7.1. Because of the temperature gradient, the particle flow occurs from the hot probe to the cold probe. When the NT is p-type, the electric current flows in the same direction as the particle flow, from the hot to the cold probe inside the NT as shown in Figure 7.1a. When the NT is n-type, the electric current flows in the opposite direction, from the cold to the hot probe as in Figure 7.1b. A voltmeter is connected to form a closed circuit and measures the electric current direction. The voltmeter can be regarded as a load resistance. Because of the current conservation, the electric current must have a circular motion. Thus, in the p-type NT, the current flows from the cold probe, through the voltmeter (load resistance), to the hot probe. Therefore, the cold probe is higher and the hot probe is lower in voltage as in Figure 7.1a. In the n-type NT, the current flows from the hot probe, through the voltmeter, to the cold probe as in Figure 7.1b. Therefore, the hot probe is higher and the cold probe is lower in voltage. Figure 7.1c is a model to be used for later discussions.

There is an easy way to visualize which probe is positive in the n-type NT [7,8]. A hot probe will accelerate electron diffusion. Thus, there will be an electron depletion under the hot probe, and this region must be positively charged. The cold probe will decelerate electron diffusion. There will be an electron accumulation under the cold probe, and this region must be negatively charged. Thus, a dipole is created such that the hot probe is positive and the cold probe is negative. The voltmeter simply detects the potential difference V created by these charges.

Usually the voltmeter has an extremely large resistance and the current through it is negligibly small. In this case, the electric field is created so that the thermal diffusion is cancelled. The thermopower measurement detects the bulk properties of the NT. In the thermoelectric power experiment, an internal electric potential caused by the thermal gradient is compared with that of the standard metal such as lead, and the potential difference is measured without practically allowing a current to flow. As long as there is no significant change in the contact properties due to temperature, the contact potential modulation in air and vacuum, if any, will cancel at the hot and the cold probes and will not influence the thermoelectric power coefficient.

The thermoelectric power of semiconducting single-walled nanotubes (SWNTs) was measured in air and in vacuum [9–13], and it has been shown that the thermoelectric power coefficient is positive in air and negative in vacuum as shown in Figure 7.2 [9] and Figure 7.2 [13], respectively. In Figure 7.2, SWNTs have been left in air and are oxidized well. Then the samples are brought into a vacuum chamber at $T = 500$ K at time $t = 0$ and the oxygen molecules are removed. At $t = 0$, the thermoelectric power coefficient is positive, indicating p-type, but as the time passes ($t > 7$ hours) and the oxygen molecules are removed, the coefficient becomes negative, indicating n-type. In Figure 7.3, SWNTs have been left in vacuum and most of the oxygen molecules are removed from the SWNTs. At $t = 0$, the SWNTs are exposed to oxygen molecules at $T = 300$ K. At $t = 0$, the thermoelectric power coefficient is negative, indicating n-type, but as time passes ($t > 70$ hours), the coefficient is positive, indicating p-type. In both experiments, it is clearly demonstrated that the SWNTs in air are p-type and those in vacuum are n-type.

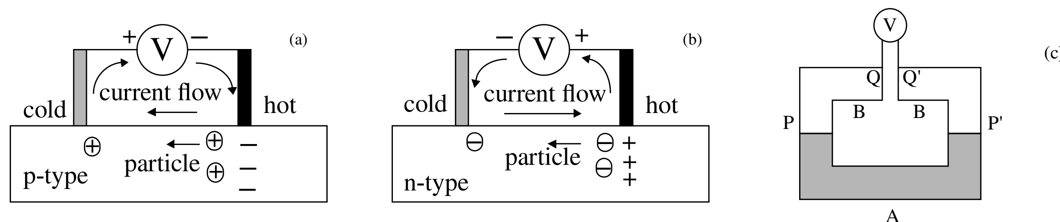

FIGURE 7.1 Schematic diagram of thermoelectric power measurement: (a) p-type case and (b) n-type case; (c) thermocoupler with a voltmeter.

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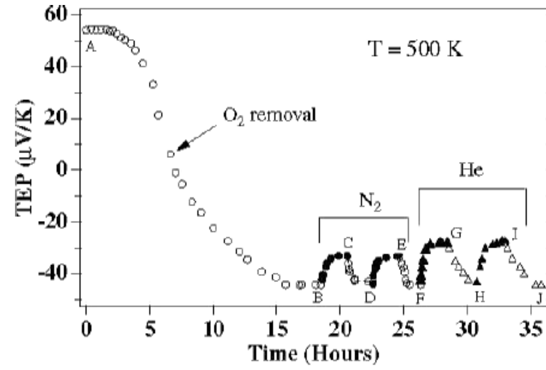

FIGURE 7.2 Thermoelectric power of an initially oxidized SWNT left in vacuum as a function of time. (Reprinted with permission from G. U. Sumanasekera et al. Phys. Rev. Lett. 85, 1096, 2000. ©2000 by the American Physical Society.)

Thermoelectric power is not related to the contact properties [6], and this is experimentally verified in the context of NT. In fact, applying the electrode contact pressure and changing the resultant contact resistance did not change the thermoelectric power coefficient [10]. This means that the thermoelectric power coefficient reflects the NT bulk properties and is not influenced by the electrode contact property change, which can be seen using the following analysis [6]. When there is no current flow, the electric field and the flow due to the temperature gradient must balance with a coefficient $e(T)$ so that:

$$dV/dx = e(T)\,dT/dx, \tag{7.1}$$

where x is a space coordinate. Introducing a function $\phi\{T(x)\}$ defined by $e(T) = d\phi/dT$,

$$e(T)\,dT/dx = d\phi/dT\;dT/dx = d\phi/dx. \tag{7.2}$$

Thus,

$$\mathrm{d}V/dx = d\phi/dx. \tag{7.3}$$

By integrating this,

$$V(x) = \phi\{T(x)\} + \text{constant}. \tag{7.4}$$

If such an electric potential $V(x)$ is generated on a ring made of two pieces with the same material, the thermal diffusion is completely cancelled in each piece and no current flows. However, if the ring is created using two different materials A and B with junctions P and P′ as shown in Figure 7.1c, the voltage E caused by the thermal gradient is measurable. Assuming that the temperatures at Q and Q′ are the same,

$$\begin{aligned} E = V(Q) - V(Q') &= \phi_A(T_Q) - \phi_A(T_P) + \phi_B(T_P) - \phi_B(T_{P'}) + \phi_A(T_{P'}) - \phi_A(T_{Q'}) \\ &= \{\phi_A(T_{P'}) - \phi_A(T_P)\} - \{\phi_B(T_{P'}) - \phi_B(T_P)\}. \end{aligned} \tag{7.5}$$

This expression indicates that the thermoelectric power is due to the bulk properties of materials A and B through ϕ_A and ϕ_B and have nothing to do with contacts P and P′, although E is determined by the contact temperatures T_P and $T_{P'}$. The fact that E depends only on T_P and $T_{P'}$ does not mean that E is determined by the contact properties only. $\phi\{T(x)\}$ is given by an integration of $e(T)$, and $e(T)$ describes how the electric field is created to balance the temperature gradient as in Equation (7.4). This is nothing but the bulk properties of an NT.

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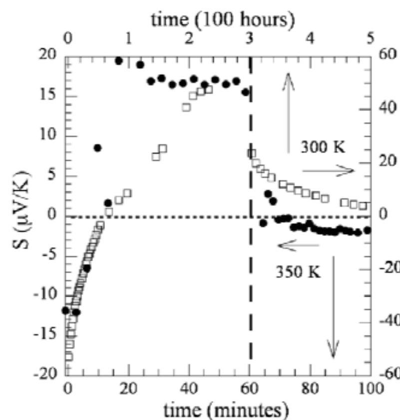

FIGURE 7.3 Thermoelectric power of an initially degassed SWNT left in air as a function of time. (Reprinted with permission from K. Bradley et al. Phys. Rev. Lett., 85, 4361, 2000. © by the American Physical Society.)

Another observation is that the thermoelectric power of A is determined *relative* to B. Usually, lead is chosen for material B, as the standard. The positive and the negative thermoelectric power coefficients simply mean that the thermopower of A is larger or smaller than that of B as seen in Equation (7.5), but in our case of the NTs, the magnitude of the thermoelectric power itself is so distinctively large (20 to 60 μV/K) that there is no ambiguity for the type of the semiconducting NT. Oxygen certainly changes the bulk properties of the NTs by inducing p-type doping. This does not necessarily mean that the oxygen molecules will remove electrons from the NT. The studies indicate either a chemisporption with a small charge transfer of about 0.1 of the unit charge [14,15] or physisorption with a negligible charge transfer in the NT-oxygen interaction [16–22]. The system consists of metallic (often gold) electrodes, oxygen molecules, and the NT, and charges can move around the system between the metal and the NT. Thus, the metal-oxygen interaction and the NT-oxygen interaction are equally important, and the system must be understood from this point of view [23].

7.1.2 Doping Characterization Using FETs

The type of a semiconducting SWNT can be clarified by building an NT FET and measuring the gate-voltage dependence [24–26]. The transistor structure and the corresponding energy-band diagram will be discussed in Section 7.3. In principle, if the transistor is normally-on, i.e., conducting with no gate voltage, V_G, a p-type is confirmed by the drain current increase with a negative V_G, and an n-type is confirmed by the drain current increase with a positive V_G. The current is influenced by the NT bulk properties and the source drain contact properties. Any difference in the NT FET characteristics in air and vacuum will be either due to the NT bulk property modulation or due to the source drain contact property modulation. In order to differentiate them, the V_G-characteristics of the NT FET need to be analyzed theoretically, including comprehensive device models.

In early experiments [27–29], the drain current was observed at $V_G = 0$ and increased at a negative V_G as shown in Figure 7.4a. This means that the NT FET had a p-channel and was normally-on in air. As V_G was increased, the NT was in the depletion mode, and the drain current decreased to a negligible level. However, a large positive V_G did not induce a finite drain current, and it was not possible to detect the inversion transport. This indicates that the source/drain contacts allow only holes to flow in and out and block out electrons.

In recent experiments with improved contacts [30–34], it is possible to observe a finite drain current in both positive and negative V_Gs as shown in Figure 7.4b. Thus, both the electron channel and the hole channel are confirmed. The NT FET is again normally-on, and the drain current increases with a negative V_G if the NT is left in air. The same measurement is repeated after the NT is annealed in vacuum and the NT is degassed. It is shown that the NT FET is at the edge of turn-on at $V_G = 0$, and the drain current

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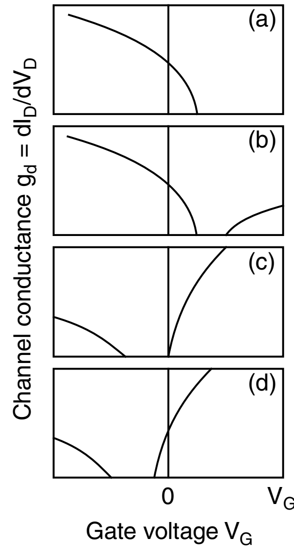

FIGURE 7.4 Schematic plots of channel conductance g_d as a function of gate voltage V_G in SWNT FET under various conditions: (a) characteristics in air at early stage of research, (b) with an improved contact in air, (c) with an improved contact in vacuum, (d) after potassium doping.

increases with a positive V_G as shown in Figure 7.4c. These results do not necessarily contradict the thermoelectric power experiments. In comparison, the characteristics for potassium doping is shown in Figure 7.4d. Alkali metals easily release electrons and dope a NT to be n-type. The NT FET is normally-on, and a positive V_G increases the drain current.

It is possible to determine a semiconductor type by examining the V_G dependence. It has to be noted, however, that the NT FET performance is influenced by the Schottky barrier modulation (contact property change) as well as the Fermi level modulation (bulk property change). Unlike the thermoelectric power measurement, the contact property change will also play an important role. For a thorough understanding, detailed modeling is warranted.

7.2 Doping Methods

In semiconductor device applications, doping and, hence, a control of the Fermi level is of great importance. Generally, there are two ways to dope a semiconductor [24]: substitutional doping and interstitial doping as schematically shown in Figure 7.5.

In substitutional doping, dopant atoms replace the lattice carbon atoms and form an sp^3 bonding in the bulk semiconductors with a diamond lattice and an sp^2 bonding in the NTs with a graphite lattice. In either case, the group III atoms are acceptors, and the group V atoms are donors. Substitutional doping has been done for an NT with boron (group III) or nitrogen (group V) recently [35,36], whereas the interstitial doping has been much more popular in the NT field, probably because of the experimental feasibility.

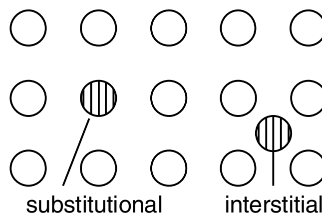

FIGURE 7.5 Schematic figure of substitutional and interstitial doping.

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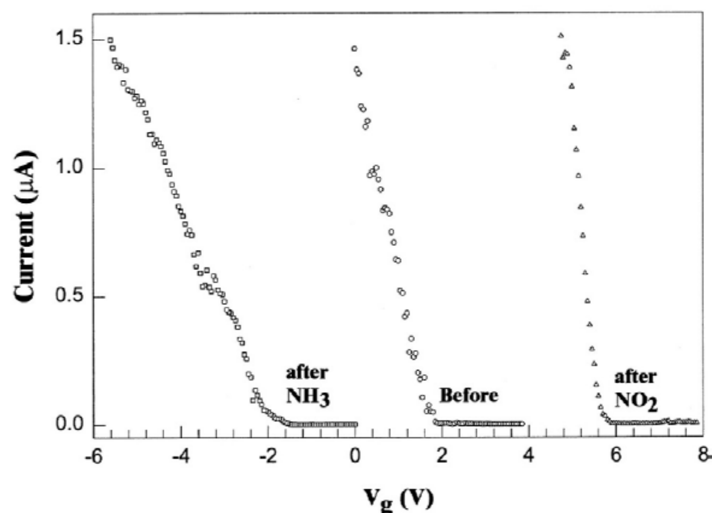

FIGURE 7.6 Drain current as a function of gate voltage for SWNT FETs: after NH_3 doping, initial, and after NO_2 doping. (Reprinted with permission from J. Kong et al. Science 287, 62, 2000. © 2000 AAAS.)

In interstitial doping, the NT lattice is unchanged, and newly introduced dopant atoms stay at the NT surface as adatoms. Dopant atoms may emit or absorb electrons depending on the relation between the highest occupied molecular orbital/lowest occupied molecular orbital (HOMO/LUMO) level of the dopant atom and the Fermi level of the NT, and it does not matter whether they are group III or group V. Materials having a deep LUMO will work as acceptors, and materials having a shallow HOMO will work as donors. It has been reported that O_2, NO_2, Br_2, and I_2 are acceptors, whereas alkali metals such as K, Cs and NH_3 are donors, and other chemicals do change the NT FET properties [37–43]. When an NT is exposed to these materials, the Fermi level rises in case of donors and lowers in case of acceptors. This was confirmed in the change in the threshold voltage of an NT FET or formation of a single-electron transistor.

As discussed in Section 7.1.2, two independent modulations, the NT bulk Fermi level modulation and the Schottky barrier modulation, contribute to the change in NT FET characteristics. One way to distinguish is to examine the channel conductance g_d vs. V_G characteristics, which is often used to determine the FET threshold voltage. The Fermi level modulation causes the horizontal shift of the entire g_d-V_G characteristics without changing the gradients of the onset points for a hole channel or an electron channel as in Figure 7.4. This can be described as a modulation of the FET threshold voltage. The Schottky barrier modulation can be seen as a change in the gradient of the onset branches in the g_d-V_G characteristics as in Figure 7.6, where the data is taken from Reference 37. Both effects are clearly seen. NH_3 has a smaller gradient, whereas NO_2 has a larger gradient in Figure 7.6. This means that the Schottky barrier for holes is higher with NH_3 than that with NO_2.

7.3 SWNT FETs

7.3.1 Basic FET Structure

Using a semiconducting SWNT, an FET has been built with significant gate modulation effects. In early experiments [27,28], a backgated structure was employed with the NT placed on a silicon substrate where the substrate surface was oxidized. Source and drain electrodes (Au or Au-Pt) were placed on the NT as shown in Figure 7.7. When the drain voltage was fixed, the drain current has a strong dependence on the applied gate voltage V_G. This is a gate modulation effect leading to signal gain.

Some fundamental properties have been studied to date, such as subband formation in the SWNT channel [44], a long-channel NT FET behavior [45], transport in a semiconducting channel [46], an effect of a defect in the NT channel [47], the use of electrolyte gate [48], and the use of large diameter NTs [49]. In addition, design principles are also discussed [50,51]. Recently, there are two areas of progress

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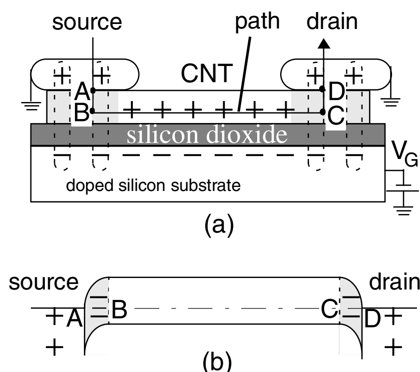

FIGURE 7.7 Backgated SWNT FET: (a) schematic structure and (b) band diagram.

in the NT FET structure. One involves placing an individual gate for each FET [31,52,53], and the other involves building a complementary FET with p- and n-channels [33,54,55].

7.3.2 Schottky Barrier at Electrode Contact

Because of the source/drain electrode contacts, there was a kink structure in the measured $g_d - V_G$ characteristics as shown in Figure 7.8 [27]. This can be explained based on the transport across the metal-semiconductor contact [56]. In the $g_d - V_G$ characteristics for a p-type NT FET, four operating points are shown with a band diagram. The drain current is negligible for (a) to (c) in the subthreshold region, and (d) is in the turn-on region. In Figure 7.8a, the position of the Fermi level is around the middle of the band gap, because the large positive V_G induces a band bending at the source and drain contacts. Because of the thermionic emission process, the drain current depends on V_G exponentially. As V_G is decreased, the SWNT band in the bulk shifts up. In Figure 7.8b, a flat band condition at the source contact is realized, and the drain current stays constant with V_G. This is the origin of the kink. Figure 7.8c corresponds to an onset of tunneling at the source contact, and the drain current starts to depend on V_G exponentially again. In Figure 7.8d, the FET is turned on. The band structure is shown with a broken line, because such a band structure can be realized only when there is inelastic scattering in the NT channel.

Recently, the SWNT FET characteristics have been studied in the context of the Schottky barrier modulation in oxidation [30,57–59]. According to Reference 54, the Schottky barrier height changes in oxidation. The g_d was observed to rise slowly at a negative V_G (V_A) and rapidly at a positive V_G (V_B) in vacuum as in Figure 7.9a, whereas in air, the g_d asymmetry flipped, i.e., g_d rose rapidly at a negative V_G (V_C) and slowly at a positive V_G (V_D) as in Figure 7.9b. This is attributed to the contact property change of the electrode and the NT in Figures 7.9c to f: at $V_G = 0$, the Schottky barrier for holes (Φ_{Bh}) was high and that for electrons (Φ_{Be}) was low in vacuum whereas Φ_{Bh} was low and Φ_{Be} was high in air. Then, g_d rose slowly at V_A because the holes started to tunnel through high Φ_{Bh}, and g_d rose rapidly at V_B because electrons started to tunnel through low Φ_{Be}. Similarly, g_d rose rapidly at V_C because of low Φ_{Bh} and g_d rose slowly at V_D because of high Φ_{Be}. In this $g_d - V_G$ experiment, the contact property modulation of the NT in oxidation was much more influential than the bulk property change, and the experimental findings were consistently explained through the Schottky barrier modulation.

7.3.3 Drain Current as a Function of Drain Voltage

In a standard metal-oxide-semiconductor FET (MOSFET) in Figure 7.10, the current saturation occurs because of the pinch-off point formation [60]. If x is the distance measured from the source to the drain, then the local carrier density is given by $q(x) = C_{ox}[V_G - V(x) - V_T]$, where C_{ox} is an oxide capacitance and V_T is an FET threshold voltage. The voltage monotonically changes from 0 at the source to V_D at the

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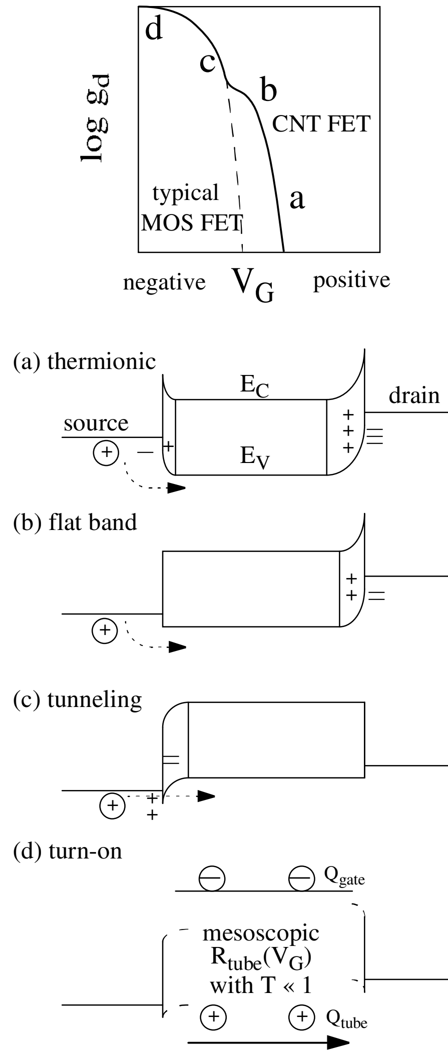

FIGURE 7.8 Schematic channel conductance g_d as a function of gate voltage V_G in SWNT FET with a kink as observed by S.J. Tans et al. [27] compared with a smooth kinkless g_d for MOSFET. (a) to (d) are band diagrams for corresponding operating points. (From T. Yamada, Appl. Phys. Lett., 76, 628, 2000. With permission.)

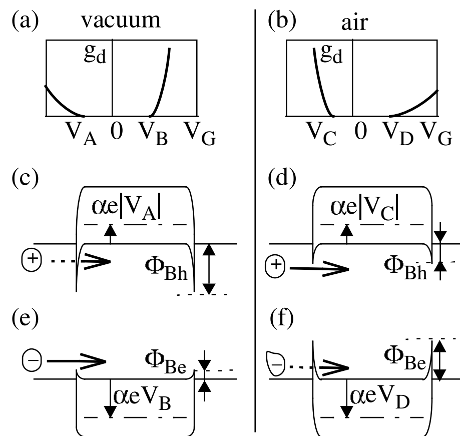

FIGURE 7.9 Schottky barrier behavior in vacuum and in air. (a) and (b) are experimental tendency of g_d as a function of V_G. (c) to (f) are band diagrams at V_A, V_B, V_C, and V_D, respectively.

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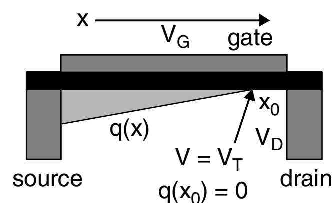

FIGURE 7.10 Pinch-off point formation in an FET.

drain. Thus, when V_D is larger than $V_G - V_T$, there exists a point X_0 where the carrier density is negligible, and this is the pinch-off point. Once this is formed, the drain current saturates, because the current magnitude is determined by the process in the inversion region between the source and the pinch-off point, which is about the channel length. Carriers passing the pinch-off point are simply swept to the drain, and there is no physical process to restrict the current flow. The saturated drain current depends on gate voltage in a quadratic way $(V_G - V_T)^2$, because both the carrier density and velocity are proportional to the gate voltage. This occurs for a long-channel FET where there is frequent carrier-carrier Coulomb scattering for the pinch-off point formation.

As the channel length reduces and becomes intermediate, the electric field between the source and the drain increases for the same drain voltage. Thus, it is possible that the threshold electric field is reached where carriers have a saturation velocity due to increasing phonon scattering before the pinch-off point is formed. This is how another type of drain current saturation occurs. The saturated drain current depends only on $(V_G - V_T)$, unlike the long-channel saturation case. Here, the carrier density depends on $(V_G - V_T)$, but the carrier velocity is the saturated velocity, which is constant and independent of the gate voltage.

When the channel length reduces further and becomes short, carrier-carrier Coulomb scattering is absent (no pinch-off point formation) and phonon scattering is absent (no carrier velocity saturation). Carriers suffer at most impurity scattering or do not suffer any scattering when traveling from the source to the drain. In this situation, the transmission picture prevails and there is no physical mechanism to cause the drain current saturation. The drain current does not saturate in these short-channel transistors.

It is experimentally confirmed that in a SWNT FET with a long-channel length of 10 µm [45], the drain current shows a saturation with a pinch-off point formation. The saturated drain current is a quadratic function of the gate voltage $(V_G - V_T)^2$, and this is the evidence of the pinch-off point formation. This means that the carrier-carrier Coulomb scattering occurs in an NT with a length of 10 µm. Such long channels are created to study basic physics of NT FETs and are certainly not suitable for nanoelectronics. In some NT FET experiments with a short-channel length of ~0.1 µm, the drain current as a function of drain voltage does not show a saturation. Thus, in these short-channel NT FETs, phonon scattering and carrier-carrier Coulomb scattering are absent. In many cases, the drain current I_D is a linear function of drain voltage V_D, but the gradient dI_D/dV_D decreases with increasing V_D in some cases [58]. Such a weak saturation often disappears when source and drain terminals are switched. This indicates that the bulk NT does not contribute to the weak saturation. From an examination of temperature dependence, it is shown that the Schottky barrier at the source contact is responsible for this. The weakly saturated current varies linearly with $(V_G - V_T)$.

7.3.4 Meaning of Drain Current Saturation in Digital Applications

Drain current saturation is important in digital applications [26]. Consider an operation of a resistor loaded inverter in Figure 7.11a. An ideal inverter will have a vertical voltage transfer characteristics as shown in Figure 7.11b, indicating that only low and high V_{out} values are possible. This is the essence of the digital applications. Because only the two signals, low and high, are allowed in the output, the inverter is quite resistant to the noise. In fact, even if there is a small deviation from the ideal low or high output,

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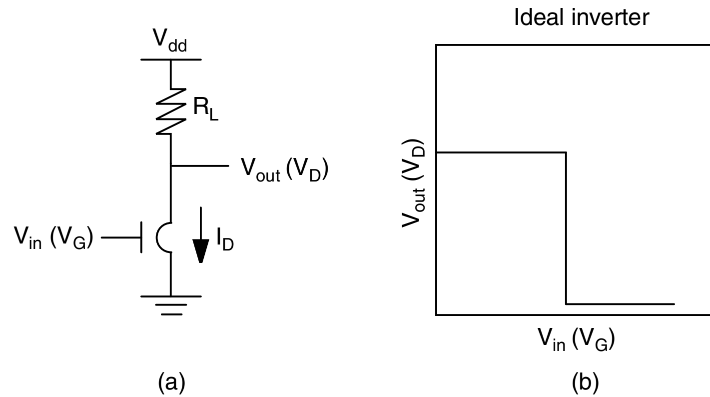

FIGURE 7.11 Resister loaded inverter: (a) circuit configuration and (b) ideal voltage transfer characteristics.

the signal is reshaped after going through another inverter. Each time the signal goes through an inverter, the unwanted noise component is removed, and this is the strength of digital circuitry.

Whether the inverter can have ideal characteristics or not depends on the performance of the FET. There are three different FETs: FET 1 in Figure 7.12a shows traditional saturation behavior, and the saturated drain current is proportional to $(V_G - V_T)^2$; FET 2 in Figure 7.12b shows a saturation, but the saturated current value is proportional to $V_G - V_T$; FET 3 in Figure 7.12c does not show any drain current saturation at all. Long-channel (~10 μm) NT FETs or individual gate NT FETs with a pinch-off point formation are like FET 1, whereas short-channel (~0.1 μm) NT FETs with at most elastic scattering are often like FET 3. Middle-channel NT FETs where the velocity saturation is relevant are like FET 2. Using a standard load line analysis, the following voltage transfer characteristics can be presented.

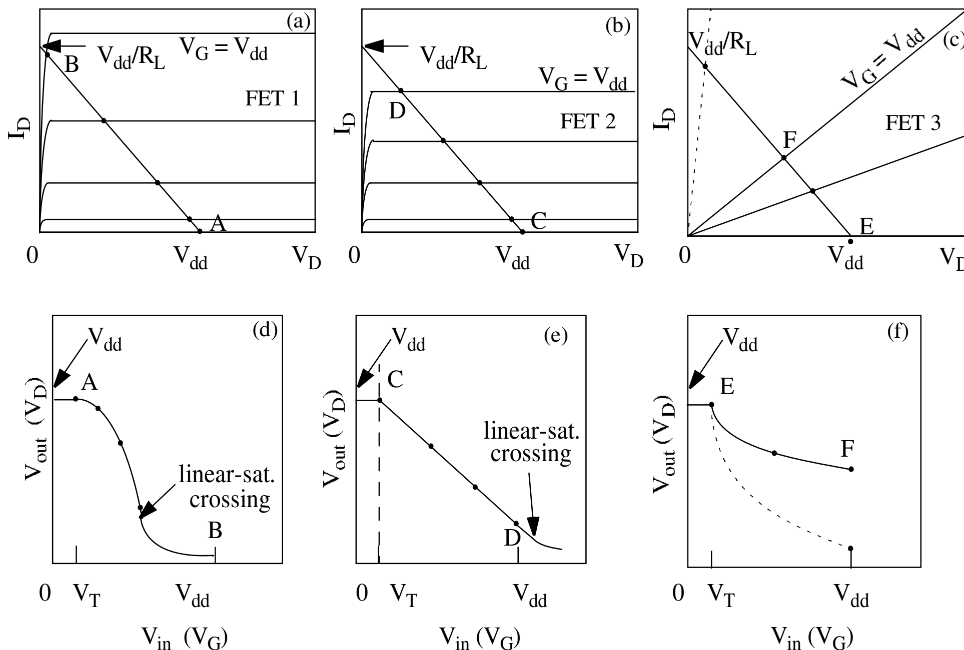

FIGURE 7.12 FET characteristics and resistor-loaded inverter performance: (a) to (c) are various FET drain current (I_D) – drain voltage (V_D) characteristics and (d) to (f) are corresponding voltage transfer characteristics.

When there is a saturation with the pinch-off point formation in Figure 7.12a, the saturated drain current lines are dense for small V_Gs but are sparse for large V_Gs reflecting the quadratic dependence, $(V_G - V_T)^2$. This is crucial in digital applications. The small change in the saturated drain current causes the convex shape of V_{out} around $V_{in} \sim V_T$ near operating point A as shown in Figure 7.12d. The saturated

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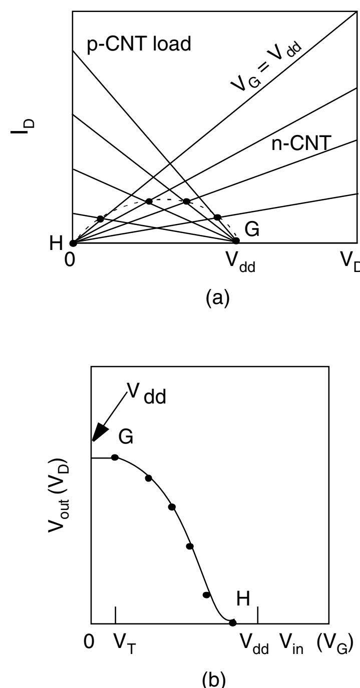

FIGURE 7.13 FET characteristics and complementary inverter performance: (a) p-channel and n-channel SWNT FET characteristics and (b) voltage transfer characteristics.

drain current increases more rapidly as V_G increases, and this brings about a rapid vertical drop in the $V_{out} - V_{in}$ voltage transfer characteristics. Near operating point B, there is a transition of the FET from the saturation mode to a linear mode, and this creates a kinklike concave-type change in the $V_{out} - V_{in}$ characteristics. The above voltage transfer characteristics are close to ideal. In Figure 7.12b, the drain current saturation is present, but the saturated drain current depends linearly on $V_G - V_T$. Although the load line intersects the drain current curve mostly in the saturation current mode like Figure 7.12a, the transition portion in the $V_{out} - V_{in}$ characteristics is mostly straight with a 45° gradient in Figure 7.12e. Thus, the inverter operational margin is narrow. Finally, when there is no drain current saturation as in Figure 7.12c, V_{out} cannot be low, and the inverter does not work appropriately as shown in Figure 7.12e.

By adopting a different circuit scheme, however, FET 2 or FET 3 can be used to build an inverter; this is necessary because micron-scale source-drain lengths are not realistic. If a complementary circuit [20,21] using a p-NT FET and an n-NT FET [39,49] is created, the inverter can have a reasonable margin, although each FET does not show an ideal drain current saturation with a pinch-off point formation. This is illustrated graphically in Figure 7.13. Performing circuit analysis with the p-NT FET as a load, the operating point will form a dotted curve like a half circle as in Figure 7.13a. This means that near the threshold voltage of either the p-NT FET (operating point G) or the n-NT FET (operating point H) the V_{out} changes slowly. Thus, a convex shape near operating point G and concave shape near operating point H are created as in Figure 7.13b, and we can achieve a reasonable inverter margin.

Experimentally fabricated complementary SWNT FETs show a more vertical transition line in the voltage transfer characteristics than a simple resistance of 45° gradient. Many nanodevices, including the NT devices, show ballistic transport in the channel and may not have a drain current saturation, but an inverter can be built with a finite operating margin. This is encouraging for the future nanoelectronics.

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7.4 Intermolecular Metal-Semiconductor SWNT Heterojunctions

By fusing metallic and semiconducting SWNTs of different chiralities, intermolecular metal-semiconductor heterojunction diodes can be created [61–66]. The diodes are expected to have a kink at the junction [65]. Indeed, rectifying current-voltage characteristics were observed for such a kink-shaped NT fused diode [66], where V_G was applied to change the carrier density in the diode and the rectifying characteristics were modulated.

This device corresponds to a gate-controlled diode known in the semiconductor electronics. The gate bias modifies the carrier density in the diode and changes the rectifying characteristics. This property itself is useful in electronics applications, but the device has been used rather in the fundamental study of the semiconductor surface potential [67,68]. For example, MOSFET energy-band structures have been studied using a gate-controlled diode [67] because of their geometrical resemblance. NT gate-controlled diodes will play the same role with respect to NT FETs. As will be shown below, the gate modulation occurs essentially the same way in these devices, resulting in the same surface potential behavior at the junction. The only difference is that NT doping is p-type in the FET whereas it is n-type in the diode.

The NT was placed on Ti-Au electrodes on a SiO_2/doped-Si substrate (backgate) as in Figure 7.14a and V_G was applied to the backgate with electrode 3 grounded [66] at 100 K. Although the circuit between electrodes 0 and 1 showed linear characteristics (110 kΩ) without noticeable V_G dependence, the circuit between electrodes 1 and 3 across electrode 2 showed rectifying characteristics with appreciable V_G dependence as in Figure 7.14b. Therefore, the right NT between electrodes 2 and 3 had to be semiconducting.

The operation mechanism can be analyzed using a one-dimensional transport modeling [69,70]. A band-diagram modeling is used here to understand how V_G modulates the diode characteristics [71]. Consider an equivalent circuit with drain current I_D and voltage V_D at electrode 1 with a linear resistor R_1 and a capacitor C_{NT} with respect to the substrate. The metallic and the semiconducting NTs meet at kink 2, and an MS junction (J_2) is formed. The semiconducting NT reaches electrode 3, and a semiconductor-metal (SM) junction (J_3) is formed. For rectification to take place, either J_2 or J_3 should be a Schottky diode and the other should be a resistive element.

The forward direction current transport occurred when $V_D > 0$ [66]. Thus, two equivalent circuits are possible [71]: J_2 is a Schottky diode with an n-type NT and J_3 is a resistor as in Figure 7.15a, or J_2 is a resistor and J_3 is a Schottky diode with a p-type NT as in Figure 7.16b. Forward and reverse turn-on voltages are introduced for a diode, V_{onF} and V_{onR}, respectively. The experimental V_G dependence is such that increasing V_G shifts both V_{onF} and V_{onR} in the positive V_D direction. Such V_G dependence is possible

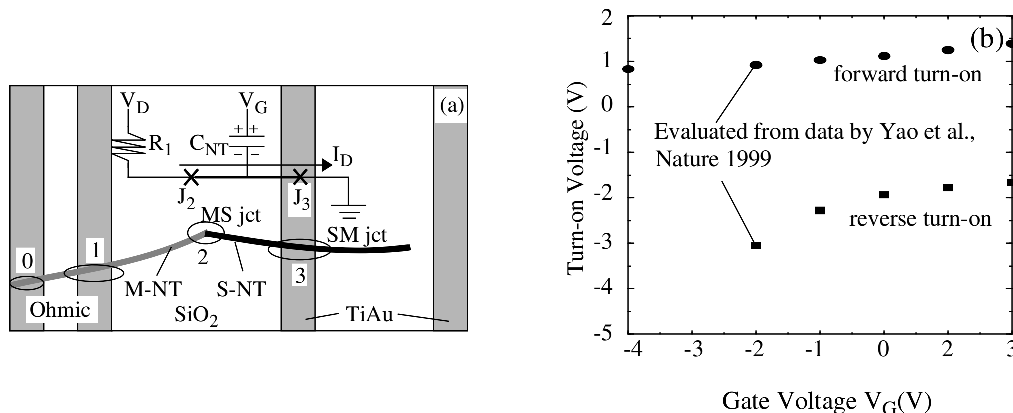

FIGURE 7.14 (a) Experimental setup of Z. Yao et al. [66] and its equivalent circuit; (b) forward and reverse on voltages (see text for definition) between electrodes 1 and 3 with V_G as a parameter at 100 K with data evaluated from Z. Yao et al. [66]. (Figure 7.14a from T. Yamada, Appl Phys. Lett., 80, 4027, 2002. With permission.)

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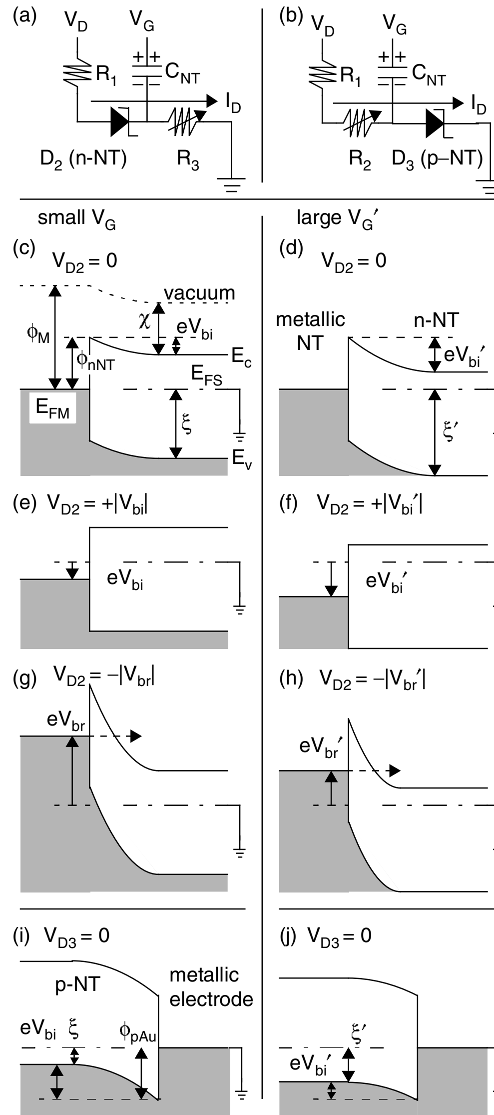

FIGURE 7.15 Rectification mechanisms: (a) equivalent circuit with a fused SWNT MS junction D_2 of n-type and an Ohmic contact R_3 with a capacitor C_{NT}, (b) equivalent circuit with an Ohmic contact R_2 and SWNT-electrode SM junction D_3 of p-type, (c) to (h) energy-band diagram for selected V_{D2}s in the n-SWNT scenario of (a), (i) and (j) energy-band diagrams for $V_{D3} = 0$ in the p-SWNT scenario of (b). Small V_G (left) and large V_G (right) cases are examined. (From T. Yamada, Appl. Phys. Lett., 80, 4027, 2002. With permission.)

with an n-NT but not with a p-NT. The band diagrams for Schottky diode D_2 of n-type in Figure 7.15a are shown in Figures 7.15c to h for selected D_2 voltages (V_{D2}s), and those for D_3 of p-type in Figure 7.15b are shown in Figure 7.15i and j for null D_3 voltage (V_{D3}). We compare small V_G (left) and large V_G (right) cases. ϕ_M is a metallic NT work function. ϕ_{nNT} and ϕ_{pAu} are Schottky barriers for electrons at D_2 and holes at D_3. E_{FM} and E_{FS} are electrochemical potentials (Fermi levels) in the metallic and the semiconducting NTs. E_c and E_v are conduction and valence band-edges with a band gap, e.g., ξ is a chemical potential $E_{FS} - E_v$ and χ is an electron affinity. V_{bi} (> 0) is a built-in voltage and V_{br} (< 0) is a breakdown voltage. e (> 0) is the unit charge.

In the n-NT scenario in Figure 7.15a, increasing V_G results in higher electron density, and ξ increases. Thus, $\xi < \xi'$, where a prime indicates a quantity at V'_G (> V_G). Because ϕ_{nNT} is independent of V_G, $V_{bi} < V'_{bi}$ as shown in Figures 7.15c and d. In the thermionic emission [24,25], $V_{onF} \sim V_{bi}$. Therefore, $V_{onF} < V'_{onF}$, as in Figures 7.15e and 7.15f. This is consistent with the experiment. The reverse turn-on occurs when $V_D \sim V_{br} = -|V_{br}|$. This is the beginning of the tunneling breakdown. The effective doping is larger

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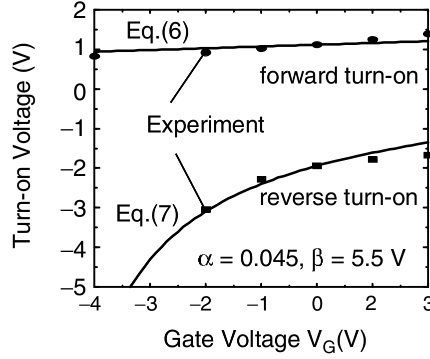

FIGURE 7.16 Comparison of modelling results Equation (7.6) and (7.7) to an experiment by Z. Yao et al. (From T. Yamada, Appl. Phys. Lett., 80, 4027, 2002. With permisson.)

for larger V_G, leading to the thinner Schottky barrier as in Figures 7.15g and h. Thus, $-|V_{br}| < -|V'_{br}|$ and $V_{onR} < V'_{onR}$. This is also consistent with the experiment. However, neither trends for V_{onF} and V_{onR} are explained by the p-NT scenario in Figure 7.15b. Again $\xi < \xi'$ but $V_{bi} > V'_{bi}$ for holes as shown in Figures 7.15i and j. Thus, $V_{onF} > V'_{onF}$. In the reverse direction, $-|V_{br}| > -|V'_{br}|$ and $V_{onR} > V'_{onR}$. Both are against the experiment. Therefore, we conclude that the rectification occurred at D_2 and the NT must be n-type.

V_{onF} and V_{onR} can be expressed as a function of V_G based on the above view. V_G causes a linear change in ξ, such that $\xi(V_G) = \xi(0) + \alpha e V_G$. The coefficient α is related to the NT state density and *NT* [71]. By the band diagram in Figure 7.15c, $eV_{bi} = \phi_{nNT} - [E_g - \xi(V_G)]$, where e is the unit charge. The forward turn-on is achieved by applying $V_{D2} = V_{bi}$ and $\Delta V_{bi}(V_G) = \alpha \Delta V_G$. The turn-on voltage modulation by V_G including the R_3 contribution in the vacuum-gap mode [72] is given [71] by

$$V_{onF}(V_G) = V_{onF}(0) + \alpha V_G, \tag{7.6}$$

$$V_{onR}(V_G) = V_{onR}(0) + \alpha V_G + (V_{onF}(0) + |V_{onR}(0)| - E_g/e)V_G/(\beta + V_G)\ , \tag{7.7}$$

where $V_G = -\beta$ is a voltage such that electrons are completely repelled, and the planar junction theory [24,25] is assumed. The choice of $\alpha = 0.045$ and $\beta = 5.5$ V recovers voltagethe experimental $V_{onR}(V_G)$ quite well as in Figure 7.16. Quasi–one-dimensional junction field [73], Fermi level pinning [74], and image potential [24,25] effects would not be relevant and are not included in our model, but they could be necessary in the analysis for finite I_D.

The gate-controlled MS diode measurements are studied, and it is shown that the rectification occurred at the kink of the NT junction and the carriers involved in the transport must be electrons, not holes. NT FETs with gold electrodes in air have p-type channels in that the transistors are already on with $V_G = 0$, and the drain current increases with a larger negative gate voltage. These two are not necessarily contradictory, because the doping effect and the Schottky barrier effect can co-exist and both influence the final device behavior. In the gate-controlled NT diode, the Schottky barrier is formed with respect to the metallic NT and is lower for electrons, whereas in the NT FETs, the Schottky barrier is formed with respect to the gold electrode and is lower for holes. For the further NT FET fundamental research, various gate-controlled NT diodes need to be studied actively, as in the silicon MOSFET research [67].

7.5 SWNT pn Junction as Esaki Diode

In the history of semiconductor electronics, people focused on tunnel diodes exhibiting negative differential resistance (NDR) as shown in the current-voltage characteristics in Figure 7.17, when three-terminal transistors were not fabricated reliably. With a device having an NDR and a gyrator allowing a signal to flow in a designated circulation direction (like a traffic rotary), it is possible to create a signal

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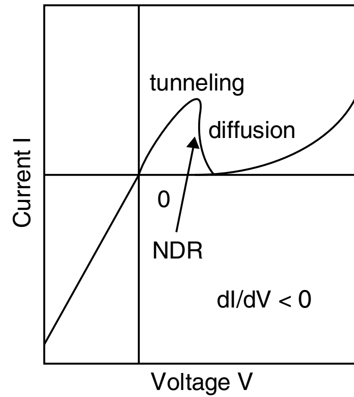

FIGURE 7.17 Current-voltage characteristics with a negative differential resistance (NDR).

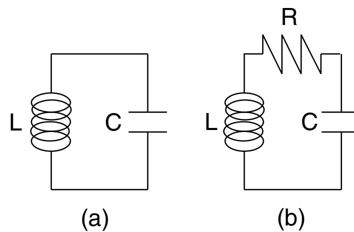

FIGURE 7.18 (a) LC and (b) LCR circuits.

amplifier [75]. The operation of such an amplifier is equivalent to that of a transistor. Another application is to use it for an oscillator circuit. An *LC* circuit with an inductance *L* and a capacitance *C* in Figure 7.18a has a resonance frequency of $\omega = (LC)^{-1/2}$. If a resistor *R* is added to the loop and an *LCR* circuit is formed as in Figure 7.18b, the resonance frequency is modulated to $\omega = (R^2 - 4L/C)^{1/2}/2L$ and the oscillation damps by $exp(-Rt/2L)$ with *t* the time. If $0 < R < 2(L/C)^{1/2}$, the oscillation will decay exponentially with time. If $-2(L/C)^{1/2} < R < 0$, however, it is expected that the oscillation grows in time. This is an oscillator generating an AC signal with a DC bias and such a negative *R* can be achieved with a device with the NDR. Because of these two major applications, NDR devices have been attracting a lot of attention historically in electronics.

An Esaki diode [76–78] belongs to this tunnel diode family with an NDR. The structure is simply a highly doped pn junction, denoted by p^+n^+, and because of this feasibility in fabrication. The NDR occurs in the forward direction. There is a bias point where the tunneling becomes maximum, and these characteristics are superimposed for a usual pn junction forward bias characteristics — larger diffusion current for increasing the bias voltage, as shown in Figure 7.17. The physical mechanism for this behavior is visualized in the band structure below.

A SWNT Esaki diode has been fabricated experimentally [43]. An NT is placed on a SiO_2/Si substrate. After placing source and drain electrodes, the drain current is measured as a function of the gate voltage. The entire NT is unintentionally doped to be p-type in air, and this is confirmed in the normally-on characteristics and the increasing drain current with a negative gate voltage. Then a half of the NT in the source side is covered by polymethylmethacrylate (PMMA), and a half of the NT in the drain side is exposed. The exposed side is doped with potassium. The potassium has a very shallow work function and dopes the NT to be n-type. Because of this initial doping difference, the source side consistently has a higher hole density and a lower electron density than the drain side, regardless of the gate voltage. The drain current as a function of the gate voltage shows that a finite drain current flows when $-12\ V < V_G < -7\ V$ and $-1\ V < V_G$, as shown in Figure 7.19A. The drain current is zero elsewhere. This is because the band structure of p^+n junction is effectively achieved for $V_G < -12$ V, p^+n^+ for $-12\ V < V_G < -7$ V,

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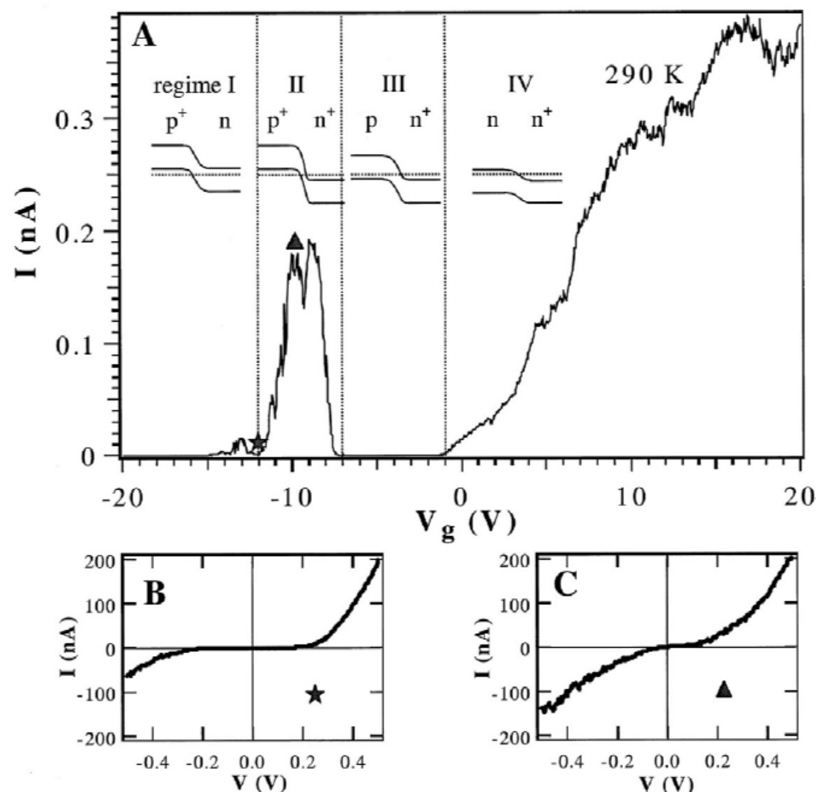

FIGURE 7.19 Experimental SWNT Esaki diode drain current vs. gate voltage: I-IV are corresponding band diagrams. (Reprinted with permission from C. Zhou et al. Science 290, 1552, 2000. ©2000 AAAS.)

pn^+ for $-7\text{ V} < V_G$, and nn^+ for $-1\text{ V} < V_G$. The p^+n^+ junction is conductive. The Fermi level in the p^+ is below the valence band top, and the Fermi level in the n^+ is above the conduction band bottom. The electrons can tunnel either from p^+ to n^+ or from n^+ to p^+ because they can find post-tunneling states in either case. The junction nn^+ is also conductive because it is Ohmic without any rectification.

It is interesting to note that after the potassium doping, the source side of the junction is no longer p-type but n-type, when $V_G = 0$. When the potassium doping is ample, there are so many electrons introduced in the NT system that some electrons are introduced even in the PMMA covered region, too. The uniform NT in air is most likely p-type, but this does not mean if the NT is partially doped n-type that the rest can remain p-type. Thus, it is critical that the experiment uses the backgated structure to manipulate the Fermi level of the NT system. Without the backgate, the resulting NT junction would be simply nn^+, which is nothing but an ohmic junction and does not show the Esaki behavior of negative differential conductance.

The NT p^+n^+ junction works as a standard silicon Esaki diode, showing an NDR as in Figure 7.20A. Electrons tunnel through from the grounded source of p^+ region to the drain of n^+ region in the reverse direction with a negative drain voltage, where the built-in voltage is increased, as in Figure 7.20B. In the forward direction with a positive drain voltage, the built-in voltage is reduced and electrons tunnel from the n^+ region drain to the p^+ region source, as in Figure 7.20C. When the drain voltage is increased, the built-in voltage is further reduced and electrons in the drain cannot find states to which they can tunnel, or the Fermi level in the drain corresponds to the band gap of the source, as in Figure 7.20D. This unavailability of post-tunneling states is the origin of the negative differential conductance and has been experimentally observed using the NT p^+n^+ junction. The built-in voltage with the further increase in drain voltage is so small that it cannot prevent an electron diffusion from the source and the hole diffusion from the drain, as in Figure 7.20E. This is the scenario of the Esaki diode and has been clearly observed in the experiment.

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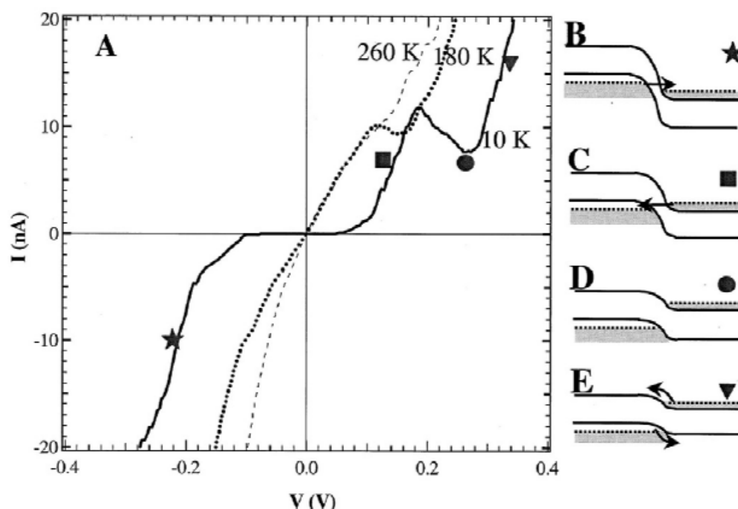

FIGURE 7.20 Experimental SWNT Esaki diode drain current vs. drain voltage characteristics. (Reprinted with permission from C. Zhou et al. Science 290, 1552, 2000. ©2000 AAAS.)

7.6 Single-Electron Tunneling Devices Using SWNTs

Single electron tunneling (SET) devices [79–82] have been studied from physics and electronics points of view. NTs have a narrow diameter, and when contacted to an electrode the overlap area is naturally small without any specific microfabrication, resulting in an extremely small capacitance C (e/C typically ranges from ~10 mV to ~1 V, with e the unit charge). This is a significant advantage of NTs in the SET device applications.

In this section, an emphasis is placed on how the current-voltage characteristics change with the device component parameters. At an early stage, two-terminal SET devices had been examined in the study of correlated tunneling in time or in space. Recently, three-terminal SET devices have been studied, where the SET characteristics can be modulated with the gate bias. There are two important phenomena related to the gate-controlled SET operation: the Coulomb oscillation and the Coulomb diamond formation. The familiar source, drain, and gate are still used to distinguish the terminals in the SET devices. In applications, an SET device is brought to a certain operation point by applying a designated bias or inducing a designated charge on an appropriate part of the device. An input is applied as the source-gate voltage and an output is obtained as the source-drain voltage, which is the same as the conventional FETs, although the current-voltage characteristics are different from those of the conventional FETs.

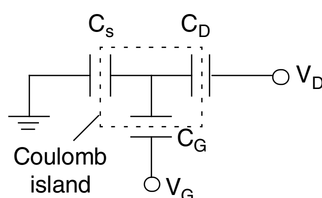

FIGURE 7.21 Equivalent circuit with a tunneling source capacitor, a tunneling drain capacitor, and a usual insulating gate capacitor.

7.6.1 Coulomb Oscillation

When a device structure is small so that the charging energy is comparable with the thermal temperature, the Coulomb blockade [79–82] often occurs. SWNT FET structures operating at a low temperature sometimes exhibit a periodic oscillation of the drain current as a function of gate voltage, known as

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Coulomb oscillation [82], a form of the Coulomb blockade phenomena. An idealized circuit for Coulomb oscillation is given in Figure 7.21. Two capacitors in series represent the source and the drain contacts, and the central island is coupled to the gate capacitance through gate modulation effect. The energy level in the central island is continuous in a long NT but is discrete in a short NT. We will see a conductance peak condition using a method developed in Reference 81.

The probability $P(N)$ for the central island to have N particles is given by

$$P(N) = \text{const} \times \exp(-[F(N) - NE_F]/k_B T), \quad (7.8)$$

where $F(N)$ is the free energy of the central island and T is the temperature [81]. If only one value of N minimizes the thermodynamic potential $\Omega(N) = F(N) - NE_F$, then the system will prefer that single N, and there will be no conductance because the number of particles in the central island cannot change. However, if two values, i.e., N and $N+1$, minimize the thermodynamic potential, $\Omega(N) = \Omega(N\text{-}1)$, then the system can allow a finite current flow with a small applied voltage because the central island can have states N, $N\text{-}1$, N, $N\text{-}1$, N, $N\text{-}1$,…, etc. $\Omega(N) = \Omega(N\text{-}1)$ gives

$$F(N) - NE_F = F(N\text{-}1) - (N\text{-}1)E_F. \quad (7.9)$$

In the low-temperature limit, the free energy $F(N)$ is the ground state energy $U(N)$ of the island. Thus, the current peak appears when

$$U(N) - U(N\text{-}1) = E_F \quad (7.10)$$

for some N. The role of the gate voltage is to change the functional form of U continuously and change the N value satisfying this relation. $U(N)$ is given by integrating $\phi(Q) = -Q/C + \phi_{ext}$ from 0 to $-NE$.

When the discrete energy separation in the island is much smaller than the nanotube charging energy, which is usually a good approximation for metallic islands with a reasonable size, we have

$$U(N) = (Ne)^2/2C - Ne\phi_{ext}. \quad (7.11)$$

The gate voltage is related to ϕ_{ext} by

$$\phi_{ext} = \text{const} + \alpha V_G, \quad (7.12)$$

where α is a capacitance ratio of the system. Now, the current peak condition can be rewritten by

$$(2N\text{-}1)e^2/2C = E_F + e\phi_{ext}. \quad (7.13)$$

Thus, the period in V_G is $e^2/\alpha C$.

When the discrete energy separation is comparable with the Coulomb-charging energy, the discreteness of the energy comes into the expression $U(N)$.

$$U(N) = \Sigma E_p + (Ne)^2/2C - Ne\phi_{ext}, \quad (7.14)$$

where the first term is a summation of the N single-electron energies in the ascending order measured from the bottom of the conduction band. Thus, the current peak condition is rewritten as

$$E_p|_{p=N} + (2N\text{-}1)e^2/2\text{C} = E_F + e\phi_{ext}. \quad (7.15)$$

Thus, the period in V_G has a doublet structure, with a spacing alternating between e^2/αC and $(\Delta E_N + e^2/C)/2$, where ΔE_N is the relevant discrete energy separation. There are two remarks. The spin degeneray is lifted by the charging. Equation (7.15) predicts the current peak locations, but cannot predict the conductance, which requires information of the tunneling rates.

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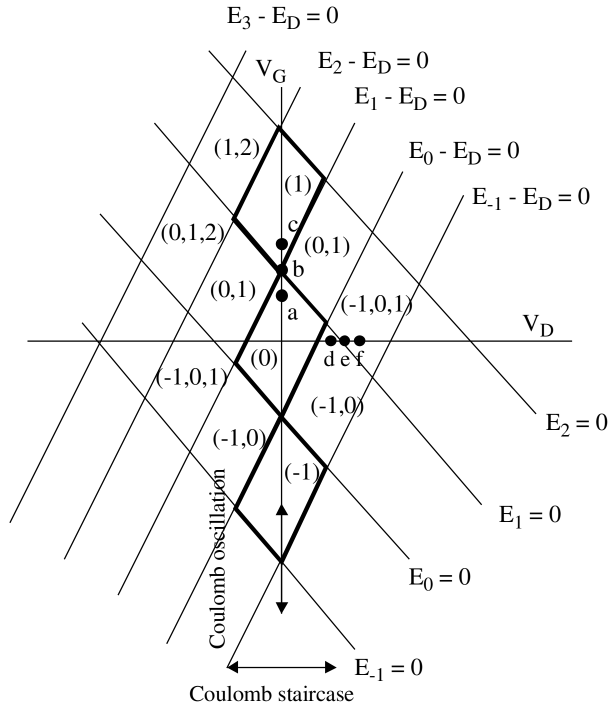

FIGURE 7.22 Coulomb blockade conductance plotted in V_G-V_D plane. Thick parallelograms are Coulomb diamonds with null conductance inside.

7.6.2 Coulomb Diamonds

In some cases, a plot is made for V_D-V_G plane, and the drain current or conductance is shown for this two-dimensional plane, as in Figure 7.22. We will disregard the discreteness of energy levels in the island for simplicity, but it will be incorporated in the same way as above. The boundaries for a finite current or conductance and zero current or conductance are parallelogram and are often called the Coulomb diamond. We will evaluate the ground-state system energy gain when an electron tunnels from electrode i ($i = S$, D, or G) to the island, where the number of electrons change from N-1 to N [83,84]. The battery loses eV_i; the island gains $e\,\Sigma C_j V_j/C$ with a summation taken for S, D, and G and $C = C_S + C_D + C_G$; and the Coulomb energy gain is $U(N)$-$U(N\text{-}1)$. The resultant ground-state system energy difference $\Delta(N, N\text{-}1)$ is given by

$$\Delta(N, N\text{-}1) = U(N) - U(N\text{-}1) - e\,\Sigma C_j V_j/C + eV_i. \tag{7.18}$$

By introducing new variables

$$E_N = U(N) - U(N\text{-}1) - e\,\Sigma C_j V_j/C, \tag{7.19}$$

$$E_i = -eV_i, \tag{7.20}$$

we have

$$\Delta(N, N\text{-}1) = E_N - E_i. \tag{7.21}$$

If this is negative, then tunneling from electrode i to the island certainly reduces the system energy and is preferred. If positive, oppositely tunneling from the island to electrode i reduces the system energy and is preferred. In the low-temperature limit, the ground-state system energy is equivalent to the free energy and tunneling absolutely occurs when this energy is negative, and the tunneling does not occur

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when this energy is positive. As usual, we take the source to be grounded ($V_S = 0$). In the $V_D - V_G$ plane, we have a series of boundary lines, which are $E_N - E_D = 0$ and $E_N = 0$, as shown in Figure 7.22.

The thick boundaries are the so-called Coulomb diamonds. Inside the diamonds, the conductance is 0. By taking $V_D \sim 0$ and scanning V_G, we will see a Coulomb oscillation. In fact, the drain current is finite only at the corners of the diamonds on the V_G axis and is 0 elsewhere. The oscillation period is e/C_G. Comparing with the previous discussion, $\alpha = C_G/C$. By fixing V_G and scanning V_D, we will see Coulomb staircase. We will see each case more in detail, considering a few operating points in the $V_D - V_G$ plane.

Operating point (a) is inside the diamond with a preferred number of electrons being 0. In fact, if the number of electrons is different from 0, the lacking or excess electrons will tunnel into or out of the island and the preferred number of electrons is reached as indicated in Figure 7.23a. For example, if the initial number is –2, then incoming tunneling is preferred as an arrow indicates, either from the source or from the drain, because $E_{-1} < 0$ and $E_{-1} - E_D < 0$. Thus, the number is –1, and incoming tunneling is still preferred as an arrow indicates because $E_0 < 0$ and $E_0 - E_D < 0$. When the number becomes 0, then it is a steady state. $E_0 < 0$, $E_0 - E_D < 0$, $E_1 > 0$, and $E_1 - E_D > 0$ means no incoming or outgoing tunneling is preferred. A similar procedure is possible if the initial number is positive.

Operating point (b) is shared by a diamond with a preferred number 0 and another diamond with a preferred number 1. Thus, the number of electrons can fluctuate between 0 and 1 and the current flows. This situation is explained in Figure 7.23b, where $V_D = 0^+$ is assumed. Now, let us assume that the initial number of electrons is –1. Then the incoming tunneling is preferred, and an electron is added to the island either from the source or from the drain. Now the number is 0. The incoming tunneling from the source is preferred because $E_1 = 0^-$, although the incoming tunneling from the drain is not since $E_1 - E_D = 0^+$. Thus, an electron tunnels from the source and the number is 1. Then, the outgoing tunneling from the drain is preferred because $E_1 - E_D = 0^+$. The electron will not tunnel to the source because $E_1 = 0^-$. Thus, we have an oscillation of the number of electrons 0, 1, 0, 1…, etc. This fluctuation gives a finite current.

Operating point (c) is similar to operating point (a). The only difference is that the preferred number is 1. Again, whatever the initial number is, the necessary number of electrons tunnel in or out through the source and the drain, and the final preferred number of 1 is reached, as in Figure 7.23c. There is no current flow.

Thus, by changing V_G at $V_D = 0$ and moving operating points from (a) through (b) to (c), we have a finite drain current only at point (b). A similar procedure repeats every time we cross a corner of a parallelogram, whereas the current is zero inside the parallelogram. This means a periodic oscillation of the drain current as a function of gate voltage and is known as the Coulomb oscillation.

By comparing operating points (d), (e), and (f), we can see how the Coulomb staircase occurs. At point (d), the preferred numbers of electrons are –1 and 0, as shown in Figure 7.23d. Let us start with no electrons on the island. An electron tunnels out from the island to the drain, and the number of electrons is –1. Then, an electron tunnels in from the source to the island, and the number of electrons is 0 again. This cycle is repeated.

At points (e) and (f), double the drain current flows because two electrons flow at once, as shown in Figures 7.23e and f. Let us again start with –1 electrons on the island. An electron tunnels in from the source to the island. Now the number of electrons is 0. This is not a stable state. Another electron tunnels in from the source of the island, and the number of electrons is 1. Then, an electron tunnels out from the island to the drain, and the number of electrons is 0. This is not a stable state, either. Another electron further tunnels out from the island to the drain, and the number of electrons is –1. This cycle is repeated. Comparing with point (d), double the drain current flows because two electrons tunnel successively. As the drain voltage increases, the drain current increases as a step, because each time the operating point crosses a parallelogram boundary the number of tunneling electrons increases by one. Depending on the value of gate voltage, the drain current may not be constant, but may change with the drain voltage on a step of the Coulomb staircase.

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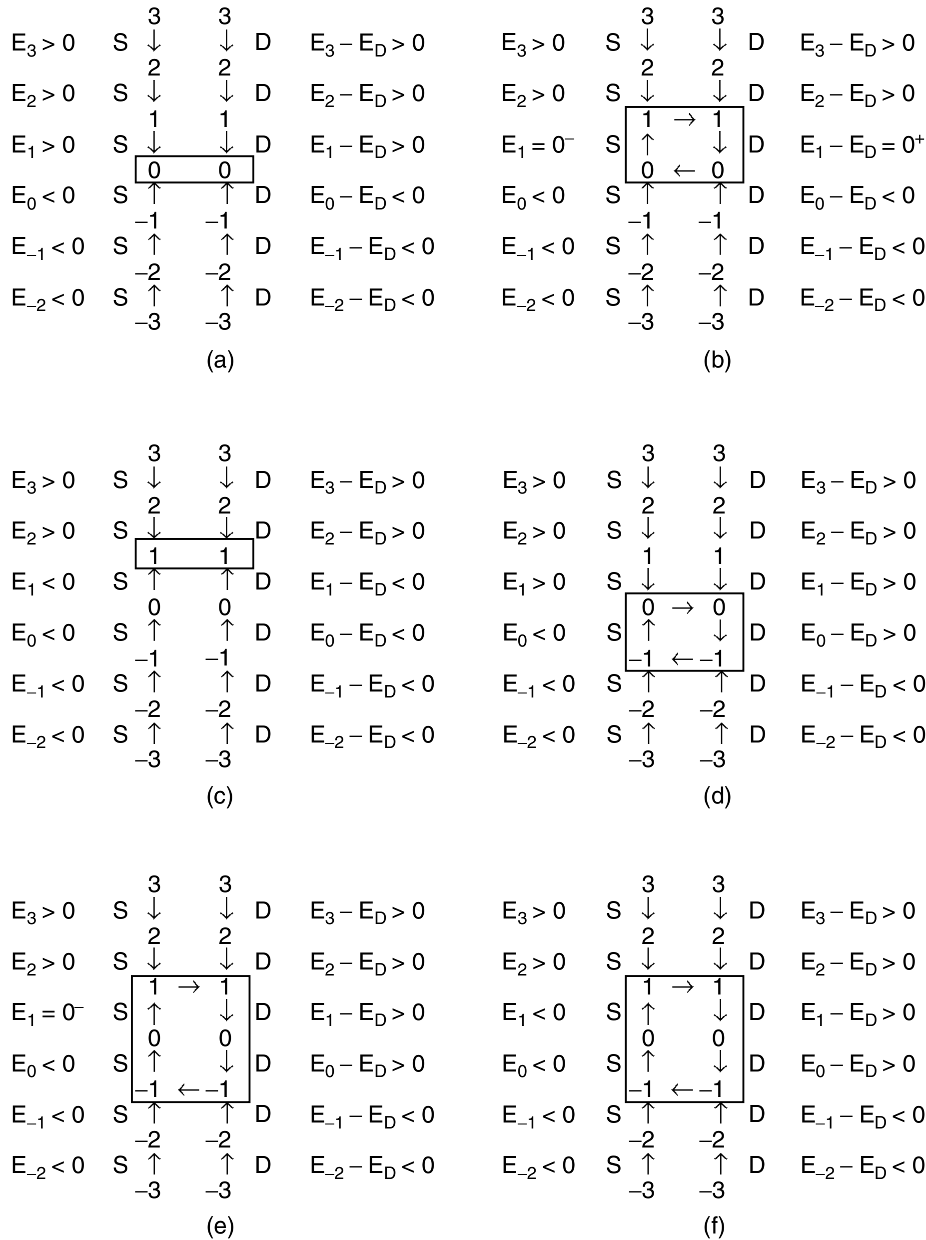

FIGURE 7.23 Number of electrons on the Coulomb island and its thermodynamically stable states for operating points (a) to (f).

7.6.3 SET Device Experiments Using SWNTs

There are many reports on the SET devices using SWNTs [34,41,43,85–96]. SWNT FETs at low temperature exhibit Coulomb diamonds in the $V_G - V_D$ characteristics, but experimentally observed diamonds often have a sawtooth structure [34,43], with a superposition of many small parallelograms. This indicates that there are multiple Coulomb islands connected in series in the channel, and multiple periods are superimposed. Similar irregularity has been observed in an NT pn junction structure [41]. We expect that there is one large NT island between the source and the drain. For various reasons, there will be random potential barriers and the large NT island is further divided. If this happens, then each island will create Coulomb diamonds. Because these islands are connected in series and no current flows inside the diamonds, the resultant Coulomb diamonds for the entire circuit will be a union of these diamonds. Thus, we will see a sawtooth structure.

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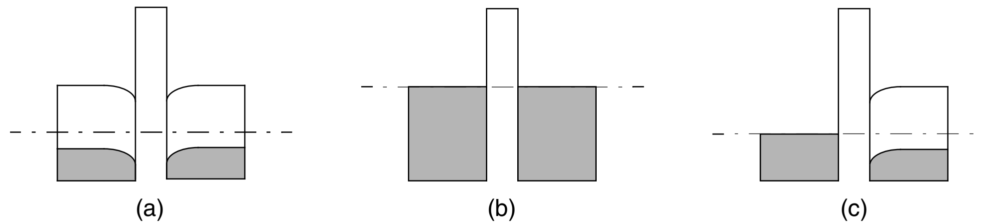

FIGURE 7.24 Band diagrams for (a) semiconducting SWNT-semiconducting SWNT (SS), (b) metallic SWNT-metallic SWNT (MM), and (c) metallic SWNT-semiconducting SWNT.

There are a few possible physical mechanisms for the formation of multiple islands. One mechanism is an impurity-induced potential barrier [43]. When dopants such as alkali metal atoms are introduced to the NT, they will not be uniformly distributed. A potential barrier will be created where the dopants are accumulated, and this will divide the NT into multiple islands. Another mechanism is the formation of pn junction near an electrode contact. In air, the Schottky barrier at an electrode contact is high for electrons and low for holes. This tends to let an end of the NT be p-type through the Schottky barrier modulation in air and oxygen doping. With an application of a large positive gate voltage, the central part of the NT is n-type. Thus, pn junctions are formed at both ends, with small p-islands. Depending on whether the NT is far enough to the electrode, the p-islands will or will not work as Coulomb islands. In Reference 41, the source and the drain contacts are not symmetric, and only one side of the p-region works as a Coulomb island. At a large positive gate voltage, the authors observed superimposed sawtooth Coulomb islands with two different Coulomb oscillation periods, whereas at a negative gate voltage they observed usual Coulomb islands with a single period, because the entire NT remained in p-type and there was one large island. A sawtooth structure was dominant in both p-type and n-type cases, and this suggests that a small Coulomb island was made probably because of the impurity barriers.

Regular Coulomb diamonds have been observed using metallic NTs. Reference 96 reports an extremely large Coulomb-charging energy in the NT field. A pair of potential barriers are introduced on a metallic NT by creating artificial defects with a chemical process, and the NT is placed on the SiO_2/Si substrate. The defects create a Coulomb island of 1~2 nm feature size, corresponding to the Coulomb energy of 400 meV or 5000 K. Thus, the room temperature operation is quite stable, and nearly ideal Coulomb islands are observed. There was an experiment with a metallic NT using the same source drain electrode geometry of an NT FET, and regular diamonds with a single Coulomb oscillation periodicity are observed. A Coulomb island is made between the source and the drain electrodes, and the period is consistent with it.

7.7 Other Semiconducting SWNT Devices

SWNT junctions have been fabricated by crossing two independent SWNTs [97]. The conductance is large in homojunctions — 0.01 to 0.06 e^2/h for semiconductor-semiconductor (SS) junctions and 0.086 to 0.26 e^2/h for metal-metal (MM) junctions — but is small in heterojunctions — 2×10^{-4} e^2/h for metal-semiconductor (MS) junctions where h is the Planck constant. The two NTs are slightly separated via a van der Waals interaction (0.34 nm), and this gap creates a potential barrier. Thus, this is a vacuum gap mode. The difference in conductance can be understood as follows. The conductance is large in homojunctions because the states before tunneling and the states after tunneling are available at the same energy level as shown in Figures 7.24a and 7.24b for the SS and the MM cases, respectively. This makes tunneling easier. The conductance is small in heterojunctions because there is a band bending in the semiconducting side, and the states for tunneling are not available at the same energy level as shown in Figure 7.24c. Rectification is observed in the current-voltage characteristics.

An NT FET may exhibit a hysteresis behavior in the $I_d - V_G$ characteristics, and this property can be used for a memory application [97,98]. Figure 7.25 schematically shows the origin of this process and the motion of positive charges. In Figure 7.25a, $V_G - V_{th}$ is 0 and the holes are just starting to be

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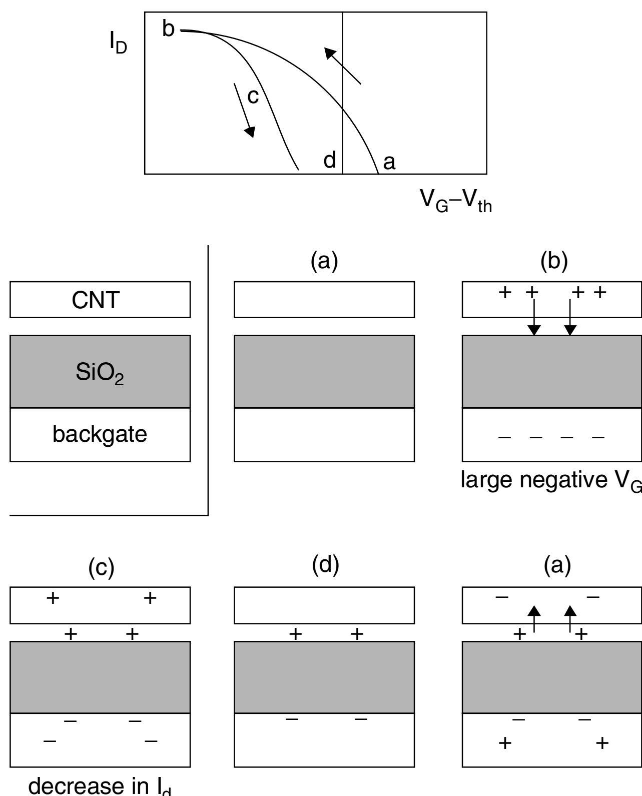

FIGURE 7.25 Mechanism for hysteresis in I_D-V_G characteristics of a SWNT FET. (a) to (d) are a real space charge distribution corresponding to the operating points.

accumulated. In Figure 7.25b, large negative V_G is applied, and a number of positive charges are induced in the NT. There are water molecules [99] between the NT and the SiO_2. In Figure 7.25c, because of the high electric field between the NT and the SiO_2, positive charges in the NT will be transferred to the water molecules. In Figure 7.25d, the positive charge remains between the NT and the SiO_2, and this increases the FET threshold voltage. The onset of hole accumulation starts at Figure 7.25a.

The silicon flash memory [100] has been quite popular recently because of its simple double-gated structure and compact size. It has a control gate and a floating gate as shown in Figure 7.26a. By charging or discharging the floating gate electronically, the FET threshold voltage is changed. There has been an effort to build an NT memory based on this flash memory mechanism, where the NT is used as an FET channel. Figure 7.26 explains the basic operation principle of the flash memory. In writing “1” in Figure 7.26a, the source is grounded, the drain is biased at 5 V, and the control gate is biased at 12 V. The FET has a pinch-off and hot electrons are created beyond the pinch-off point. These electrons can tunnel to the floating gate, and this is how the floating gate is charged. Because of this charge, the FET has a higher threshold voltage. In writing “0” in Figure 7.26b, the source is biased at 12 V, the control gate is biased at 0 V, and the drain is floating. Electrons on the floating gate will tunnel to the source, and the floating gate is discharged. This decreases the threshold voltage of the FET. In reading, V_{CGR} is applied to the control gate. Depending on whether there are electrons on the floating gate (“1”) or not (“0”), the FET will have negligible I_D(“1”) or finite I_D(“0”). In the experimental NT flash-memory operation, an appreciable threshold modulation was observed [101].

Two different modes for contact, the vacuum-gap mode and the touching mode, are proposed for a metal-semiconducting NT junction [72] realized in a metallic scanning tunneling microscope (STM) tip and a semiconducting NT [102,103]. With the tip grounded, the tunneling in vacuum-gap mode would produce a large conductance with a positive bias $V > 0$ and a small conductance with $V < 0$ for either an n-type or p-type NT, where the gap ΔV exists as shown in Figure 7.27a. The Schottky mechanism in

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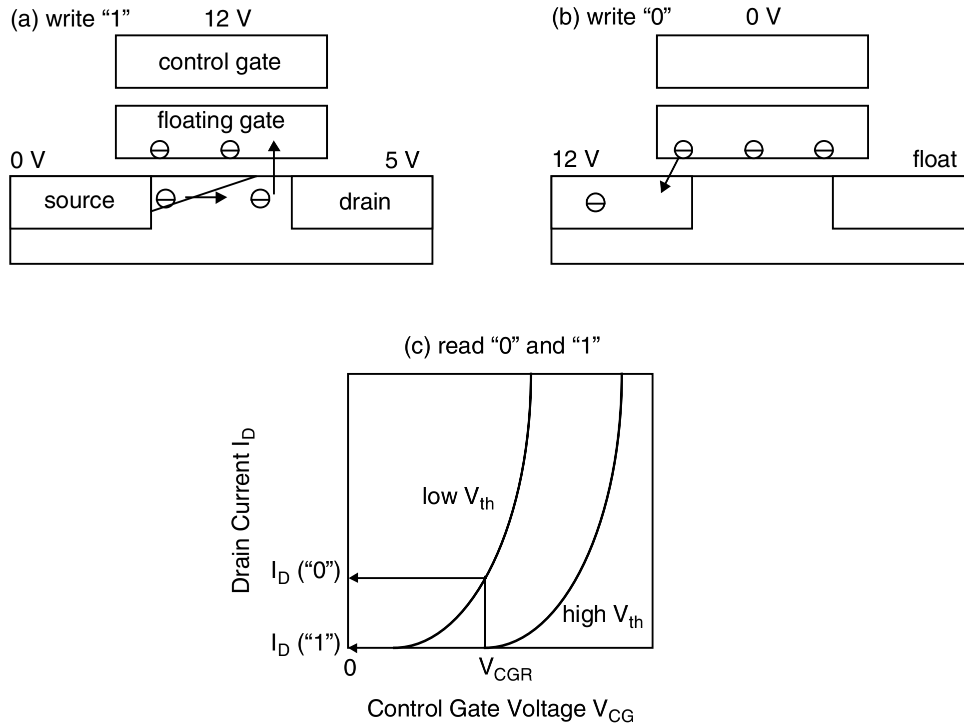

FIGURE 7.26 The principle of flash memory: (a) write "1;" (b) write "0;" (c) read.

the touching mode would result in rectifying characteristics, where the current flows only with $V < 0$ as in Figure 7.27b. Thus, the NT must be n-type. The vacuum-gap mode is schematically shown at left and the touching mode is shown at right in Figure 7.27c. These current-voltage characteristics are explained by the band diagrams. For the vacuum-gap mode, (d) is the valence band tunneling ($V < 0$), (e) is the equilibrium ($V = 0$), and (f) is the conduction band tunneling ($V > 0$). For the touching mode, (g) is the Schottky forward transport ($V < 0$), (h) is the equilibrium ($V = 0$), and (i) is the Schottky reverse transport ($V > 0$). The two observed current-voltage characteristics are entirely explained by a tip-NT contact of the two types with the above band diagrams.

In the NT production process, it is often the case that metallic and semiconducting NTs are obtained. An elegant way to obtain semiconducting NTs is reported [104]. By conducting an electric current, it is possible to burn metallic NT and obtain semiconducting NT selectively.

7.8 Transport in Metallic SWNTs

Metallic SWNTs are quasi–one-dimensional conductors. A conductance of metallic NT up to 4 μm was measured replacing a scanning probe microscope tip with an NT fiber, which was lowered into a liquid metal to establish a gentle electrical contact [105,106]. The conductance was quantized with $G_0 = 2e^2/h$ at a room temperature. Although the lowest subband was doubly degenerate in metallic NTs theoretically [1–3], the observed lowest conductance was G_0, indicating that the degeneracy was lifted. In the statistical data of conductance, the observed conductance had a strict cutoff at an integer multiple of G_0. This is because the transmission probability is limited to at most 100%, and it is impossible to go beyond it. Thus, there is a natural cutoff in the statistical data of the measured conductance at an integer multiple of G_0.

If there are scattering centers in a metallic NT, we can estimate a conductance using the Landauer-Butticker formula [107–113] and find a quantitative agreement with the experiment above. The coherent transport, including resonance tunneling, is possible in metallic NTs [114–120]. This is thanks to a good Ohmic contact between the metallic NT and the metallic electrodes. In case of semiconducting NTs, an

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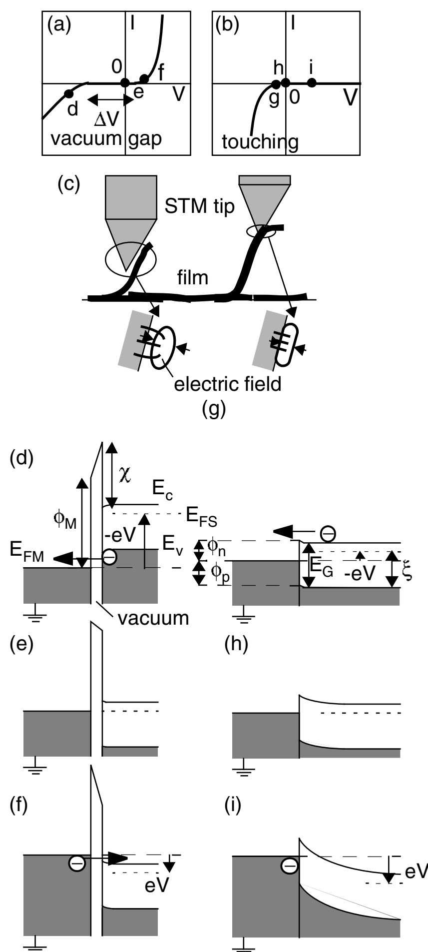

FIGURE 7.27 Vacuum gap and touching modes in the metallic tip — semiconducting SWNT. (a) and (b) the current-voltage characteristics for the vacuum-gap mode and the touching mode, respectively. (c) is the schematic showing the vacuum-gap (left) and the touching (right) mode. (d) to (f) are the band diagrams for the vacuum-gap mode. (g) to (i) are the band diagrams for the touching mode. (From T. Yamada, Appl. Phys. Lett., 78, 1739, 2001. With permission.)

Ohmic contact is not achieved easily and a Schottky barrier is often formed. In this situation, the effect of the Schottky barrier is much more influential in the current-voltage characteristics.

It is reported that when NTs are crossed, there are two different modes for crossing each other: the contact mode and the separate mode. The contact mode can conduct a lot of current, whereas the separate mode can conduct much less current [121]. The difference in a mechanical contact property is converted to a electronic transport difference and will be useful in device applications.

Metallic NTs are often discussed in the context of strongly correlated electrons [122–125], and the interplay of the many-body effects and the Coulomb interaction is discussed in Reference 125, but they are often studied in view of fundamental physics rather than device applications. They are not discussed further.

7.9 General Remarks on NanoFETs

SWNT FETs are some of the most actively studied nanoFETs and share many properties with other nanoFETs. Thus, nanoFETs in general are discussed below with the emphasis on the device-level problems. The problems related to future highly integrated circuitry with nanoFETs, such as an expected large heat dissipation from a chip beyond the present cooling technology [126], are not discussed here.

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7.9.1 Properties of NanoFETs in Comparison with Macroscopic FETs

In the present silicon-based technology, FETs play a central role in electronics. For this reason, most recent nanodevice research, regardless of the channel conduction material, focuses on the FET scheme. Here a comparison of the macroscopic FETs and nanoFETs is drawn in view of how the channel material will influence the device characteristics. Because the FETs are genuine three-terminal devices, the characteristics in response to the drain voltage and the gate voltage need to be discussed independently.

The drain-voltage characteristics show significantly different behaviors. The characteristics are strongly dependent on the channel material in macroscopic FETs, whereas the characteristics are mostly independent of the channel material in nanoFETs. In a macroscopic FET, the drain current as a function of drain voltage is proportional to the carrier mobility [60]. The mobility is proportional to the mean free time of a carrier traveling without being scattered and the effective mass of the carrier. One of the main scatterers is phonon, and the phonon properties are different from material to material, reflecting the bulk material property difference. The effective mass represents the band structure of the bulk material and is again material dependent. Adopting a different channel material will certainly result in different transport characteristics. However, in nanodevices with an ideal electrode contact, the drain current as a function of drain voltage is determined by a transmission coefficient of an electron flux flowing from the source to the drain in the Landauer-Butticker view [101–107]. In the limit of an ideal nanoFET where carriers can run ballistically from source to drain, the transmission coefficient is unity, and there is no difference among different channel materials. In reality, it is not trivial to have ideal electrode contacts, and the transmission coefficient is reduced at the source drain contacts. Depending on the channel material, the feasibility of taking an electrode-channel contact differs, and in this sense, the characteristics will depend on the contacts. It has to be noted, however, that the bulk channel material properties do not play any role in this discussion.

The gate-voltage characteristics show similar behaviors for the macroscopic FETs and nanoFETs. In both cases, the problem is reduced to how effectively carriers are induced in the channel using the gate capacitance. Thus, the characteristics are determined by the thickness and the dielectric constant of the insulating layer, which are related to the environment around the channel. Ironically, this has no direct connection to the channel material itself. Depending on the choice of the channel material, the feasibility of preparing the insulation layer may differ, but there is no essential difference for the macroscopic FETs and nanoFETs.

In nanoFETs, the properties of the bulk channel material do not influence the FET performance directly. The performance, however, is still channel-material dependent in the sense that the feasibility in creating an ohmic contact or placing an insulating layer is different from material to material. Sometimes, this indirect influence is significant. As seen in Section 7.6, the narrow geometry of nanowire channels does not need a microfabrication to create an extremely small capacitor and is highly advantageous in SET applications. These situations are unique compared with macroscopic FETs, where the bulk channel material properties are everything in the performance.

7.9.2 Forgotten Benefit of NanoFETs

When Shockley wrote a paper on an FET [60], he demanded that the FET channel be very thin compared with the channel length, so that the variation of the electric field along the channel is much less than the corresponding variation perpendicular to the channel. In other words, the dominant electrostatic problem is in the perpendicular direction to the channel, and carriers are securely confined to the thin channel so that the distance to the gate electrode is minimal and the on state and the off state of the transistor are very well distinguishable. A largest possible current ratio for on and off states is one of the basic requirements for FETs. In order to achieve this, carriers need to be placed right below the gate electrode. Confined in a thin channel layer, carriers are minimally distant from the gate electrode, and their concentration is most effectively controlled by the gate voltage. This will result in excellent transistor performance.

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As the channel length shrinks, this situation does not hold any more [24,26], and the electric field variation near the source and the drain cannot be negligible. The carriers are no longer confined to a thin layer below the gate electrode and are distributed deeper into the substrate near the source and the drain. The significant portion of the carriers is away from the gate electrode. This will cause the so-called short-channel effects. In this situation, the gate voltage cannot effectively control the carrier concentration and the transistor does not shut off well. Even if a gate voltage is applied to shut off the transistor, there is still significant drain current, and this degrades the transistor performance. This is often referred to as the reduction of threshold voltage. This is one of the serious problems the current silicon complementary MOS (CMOS) technology faces, and we are forced to engineer the channel doping to suppress these unwanted short-channel effects, but such doping control is highly challenging.

The fundamental solution is to adopt a transistor channel material that is, from the beginning, two-dimensional or one-dimensional so that the channel thickness is minimal. Nanodevices based on molecules, nanotubes, or DNAs are, from the beginning, quasi–one-dimensional and will be potentially quite advantageous in inherently suppressing the short-channel effects. In fact, nanotube FETs have shown excellent performance, which is already comparable with that of the state-of-the-art complementary MOS (CMOS) technology [59], and this is largely due to this "thin layer effect" caused by the adoption of a thin nanotube for the channel.

Nanodevices are inherently free from the short-channel-effects, and we will never face this serious problem in the future. Despite many anticipated fabrication problems in the future, it is quite meaningful to pursue nanotechnology in this context, in addition to the apparent benefit of the ultimate small size.

7.9.3 Two-Terminal vs. Three-Terminal

In electronics applications, special attention is paid to input and output electrodes. When a device has electrically independent input and output electrodes it is called three-terminal, having an input electrode, an output electrode, and a ground electrode. The electric isolation of the input and the output electrodes is essential, because otherwise the input and the output signals are mixed. Because of this isolation, in series connection of these devices, the signal can transmit only to the designed direction. Let us suppose a series connection of device A, device B, and device C such that the output of A drives the input of B and the output of B drives the input of C. In this case, the output signal of B transmits only to C, and it will never bounce back to A because of the input-output isolation. Therefore, the signal flow from A to B to C is established. A two-terminal device has only two electrodes. In the series connection of device A, device B, and device C, if the output signal of B will transmit to A as well as C because of the lack of the input-output isolation. The signal flow is not well established, and this is a serious problem in circuit applications. As is obvious here, even if a device has three electrodes, if the input and the output electrodes are not electrically isolated, it is not three-terminal.

A MOSFET is a three-terminal device, and in a most basic inverter circuit application, the gate electrode receives an input signal, the drain electrode gives an output signal, and the source electrode is connected to the ground. The gate electrode and the drain electrode are electrically isolated via a silicon dioxide layer, which is an excellent insulator, and there is no possibility for the input-output signal mixture. A Schottky diode is two-terminal, and one terminal is used for input/output and the other is used for ground. A Josephson junction diode is another example of two-terminal devices. In these diode examples, special circuitry has to be built to prevent a reverse, unwanted signal flow (from device B to device A in the example above).

Extensive circuit libraries suitable for three-terminal devices have been created; in fact, the current silicon CMOS technology relies on them. Thus, circuitry with any new devices can be immediately created as long as they are three-terminal. The new devices can be dropped in for the present MOSFETs. The situation is not this straight for two-terminal devices, because different circuit libraries than what we are using now must be developed. However, starting from scratch may not be necessary. Historically, new circuit libraries were developed for two-terminal devices [127,128]. In the 1950s, when semiconductor three-terminal devices were not very reliable but semiconductor diode devices were, "diode logic" was

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proposed and provided a circuit scheme based on the two-terminal devices only. In the 1960s, tunnel diodes were studied actively, and again suitable circuit schemes were considered. In the 1980s, Josephson junction diodes were studied. In these studies, it has been shown that "quasi-three-terminal devices" having independent input and output electrodes would be created by connecting diode elements.

In nanodevices, NTs, molecules, or DNAs are used for the device channels. All these structures are one-dimensional having two ends. Thus, without any special effort to place a third electrode, the device is inherently two-terminal. The proposal [129] to place a foundation in the diode logic scheme in the future nanoelectronics is based on this understanding. A nanosale molecular-switch 8×8 memory cell has been demonstrated toward this direction, using a cross-bar geometry memory scheme [130]. New two-terminal circuit schemes need to be developed, or three-terminal devices using nanotechnology need to be created.

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