Personal Information

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Jul 2010-present Associate Professor. University of California, Santa Cruz.
Jul 2004-2010 Assistant Professor. University of California, Santa Cruz.
Jan 1999-Jun 2003 Research Assistant. University of Illinois at Urbana-Champaign.
Aug 1998-Dec 1998 System Administrator. University of Illinois at Urbana-Champaign.
Jan 1998-Jul 1998 Computer Network Specialist. FIHOCA, S.A. (Spain).
Sep 1996-Sep 1997 System Administrator. Asertel, S.A. (Spain).
May 1995-Sep 1996 Systems Manager. Ramon Lull University (Spain).

Education

University of Illinois at Urbana Champaign: (Advisor: Professor Josep Torrellas)
2004 Ph.D. Computer Science, University of Illinois at Urbana Champaign.
Thesis: *"Chip Multiprocessor with Thread Level Speculation: Performance and Energy"*
1999 M.S. Computer Science, University of Illinois at Urbana Champaign.
Thesis: *"Memory Hierarchies in Intelligent Memories: Energy/Performance Design"*
Ramon Llull University, Spain:
1997 M.S. Computer Engineering, Ramon Llull University (Spain)
Thesis: *"Linux Kernel IEEE1284 (parallel port) Implementation"*
1994 B.S. Computer Science, Ramon Llull University (Spain)
Final project: *"ILZR, a New Data Compression Algorithm"*

Awards and Funding

- 2015, co-PI NIH Non-Invasive Magnetic Nanothermotherapy for the Resolution of Wound Biofilm Infection ($50K)
- 2015, co-PI NSF Efficient Cascode Power Supply Systems ($285K)
- 2013, PI NSF XPS Cooperative Deterministic Concurrency ($750K)
- 2013, PI NSF CSR Rethinking the Memory Hierarchy ($500K)
- 2013, Intel Gift ($10K)
- 2012, PI NSF CRI:Fast Performance, Power and Thermal Modeling for Heterogeneous System ($300K)
- 2011, PI NSF CRI: Prototyping Platform to Enable Power-Centric Multicore Research ($120K)
- 2010, AMD gift ($10K)
- 2010, PI NASA/UARC, *Dynamically Adaptable Computers for Renewable Energy Powered Data Centers* ($25k)
- 2009, SUN cash gift ($75K)
- 2008, NVIDIA cash gift ($70K)
- 2008, PI NSF CRI: IAD Temperature Measurement Infrastructure for Power, Variability, and Reliability Analysis ($275K)
- 2007, PI NSF SMA: Accurate Temperature Measurement Infrastructure and Methodology for Power, Variability, and Reliability Analysis. (co-PI are Ali Shakouri, Matthew Gutthaus, Steve Kang, and Michael Huang) ($300k UCSC + $100k Rochester)
- 2007, PI NASA/UARC, *Radiation Tolerant FPGA Processor* ($25k)
- 2007, SUN Academic Excellence Award ($110K)
- 2007, co-PI Special Research Grant from UCSC (PI is Matthew Gutthaus) ($20k)
- 2007, Xilinx University Donation Software ($8k)

- 2006, co-PI IES Berkeley/France Fund Award (co-PI is Albert Cohen) ($9k)
- 2006, PI Special Research Grant from UCSC ($12k)
- 2006, PI NASA/UARC ($50k) *Checkpointed Fault Tolerant FPGA Systems*
- 2006, PI NSF CAREER ($400k) *Understanding, Estimating, and Reducing Processor Design Complexity*
- 2006, SUN equipment (Niagara server $16k)
- 2006, Altera equipment (Stratix II DSP board $5k)
- 2006, IEEE Micro Top Picks in Computer Architecture
- 2005, PI DARPA PERCS subcontract ($20k)
- 2003, IBM Graduate Research Fellowship
- 2003, J. Poppelbaum Memorial Award, University of Illinois

Selected Publications

[1] *Section Based Program Analysis to Reduce Overhead of Detecting Unsynchronized Thread Communication*, Madan Das, Gabriel Southern and Jose Renau, ACM's Transactions on Architecture and Code Optimization (**TACO**), March 2015.

[2] *ESESC: a Simulator for Time-Based Sampling of Heterogeneous Multi-threaded Systems*, Ehsan K.Ardestani and Jose Renau, International Symposium on High Performance Computer Architecture (**HPCA**) ,February 2013.

[3] *An Energy Efficient GPGPU Memory Hierarchy with Tiny Incoherent Caches*, Alamelu Sankaranarayanan, Ehsan K.Ardestani, Jose Luis Briz, and Jose Renau, International Symposium on Low Power Electronics and Design (**ISLPED**), September 2013.

[4] *Releasing Efficient Beta Cores to Market Early*, Sangeetha Sudhakrishnan, Rigo Dicochea, and Jose Renau, International Symposium on Computer Architecture (**ISCA**), June 2011.

[5] *Characterizing Processor Thermal Behavior*, Francisco J. Mesa-Martinez, Ehsan Ardestani, and Jose Renau, Fifteenth International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), March 2010.

Students

- Current Phd: Wael Ashmawi (06-), Alamelu Sankaranarayanan (07-), Rigo Dicochea (07-), Gabriel Southern (08-), Elnaz Ebrahimi (09-), Sankara Venkateswaran (09-), Haven Skinner (11-), Rafael Trapani Possignolo (12-), Daphne Gorman (12-), Sina Hassani (13-), Akash Sridhar (14-), Meeta Singha-Verma (14-)
- Current MS: Tom Golubev (09-), Jamal Roache (13-)

Alumni:

- PhD: Javi Martinez (04-07), Cyrus Bazeghi (04-08), Sangeetha Nair (05-11), Sean Halle (04-11), David Munday (07-13), Ehsan Ardestani (08-14), Madan Das (08-15)
- MS: Shantanu Kale (05-06), Liying Su (05-06), David Brian Van Der Bokke (05-06), Suraj Narender (05-07), Angela Schmid (06-07), Matt Fischler (06-07), Melisa Nuñez (05-08), Joseph Nayfach (05-08), Keertika Singh (08-09), Michael Brown (06-11), Raj Maitra (12-12), Pranav Natesh (10-12), Ian Lee (09-12), Jason Duong (09-13), Vidyuth Srivatsaa (10-13), Christopher Hoseit (12-13), Himabindu Thota (12-13), Gregory Jackson (09-15), Ethan Papp (14-15)

Current and Past Lead Projects

Energy Efficient Designs Energy is a key metric like performance. I have several works [4, 46, 17, 32, 34, 23, 24, 25, 26, 27, 35, 36, 28] looking at different architectural techniques to reduce power consumption for core microarchitecture, memory subsystems, and overall SoC.

Thermal Measurements Our group developed the first academic project to measure thermal profiles from unmodified chips. These works [16, 12, 11, 30] pointed to several pitfalls in computer architect thermal simulations, and the design of infrared transparent heat sink solutions.

Fast Simulation Fast multicore simulation with performance, power, and thermal metrics can be very slow. These works [9, 7, 6, 5] developed sampling techniques to allow multithreaded and thermal simulations to work efficiently.

ESESC ESESC is an open source architectural simulator based on SESC. Both simulators are designed and maintained by my research group. They include the latest advances in statistical sampling to allow detailed performance, power, and temperature results with modern multicores. SESC and ESESC are cited by over 50 papers per Year since 2009. Different parts of the simulator have been verified against several real (RTL) implementations.

Complexity Metrics Processor design and implementation is a complex and resource intensive enterprise. Ideally, designers should be able to quantify the design time implications of their architectural proposals, in order to make more educated decisions and design trade offs. These works [19, 15, 49, 48, 10] address the lack of quantitative methodologies to estimate processor design time.

Complexity Effective Designs Coupled with complexity metrics, works [8, 13, 14] explore architectural techniques and potential benefits of tolerating buggy processors.

Thread Level Speculation Thread Level Speculation (TLS) has the potential of extracting parallelism without the need of programmer support. These works [22, 21, 20, 18, 33] focused on the compiler and architecture solutions to have an efficient implementation. More recent work [29] shows compiler algorithms to improve thread escape analysis that allow less overhead in many parallel tasks like versioning or data race detection.

GlobalFoundries 28nm MURN Flow I have been leading a project with GlobalFoundries and UC San Diego to develop an academic tapeout flow for 28nm. The flow includes all the synthesis and specefications scripts to implement an on-chip network, package, and bringup board so that other academic projects can start with a lower cost.

Huawei Consulting 2013-2015 I have done several tasks at Huawei but the more important were to implement a golden reference memory model (SystemVerilog and DPI), create architectural timing models for memory subsystem, create the high level simulation infrastructure for future processor generations, many architectural proposals, and review the synthesis flow and architectures designed. The goldmem reference model is used for future ARMv8 cores. The verification flow handles coherence and release consistency and interfaces back to the ISA model so that any parallel application can be checked.

Imagination Consulting 2015 I ported ESESC to MIPS64R6, created a performance model to match some of the MIPS cores, and analyze and propose Javascript specific optimizations.

Starting Projects

Fluid Pipelines Fluid Pipelines is a new methodology and a programming language to significantly reduce processor design time. The Fluid Pipeline infrastructure and a methodology will enable automatic correct-by-construction transformations that avoid costly design and verification. It automatically adds and removes pipeline stages; automatically changes the number of ports in storage structures and to allow pipeline stage replication; automatically selects the best power domain areas and actuators; and reduces safety margins with time speculation without requiring costly pipeline flushes.

Going Live Improve processor design flow to provide Live feedback to the user. Focusing on small incremental changes and always keeping the feedback in few seconds.

Publications

Conferences

[1] *SRAM Voltage Stacking*, Elnaz Ebrahimi, Rafael Trapani Possignolo, and Jose Renau, International Symposium on Circuits and Systems (**ISCAS**), May 2016.

[2] *Analysis of PARSEC Workload Scalability*, Gabriel Southern and Jose Renau, International Symposium on Performance Analysis of Systems and Software (**ISPASS**), April 2016.

[3] *LiveSim: Going Live with Microarchitecture Simulation*, Sina Hassani, Gabriel Southern and Jose Renau, International Symposium on High-Performance Computer Architecture (**HPCA**), February 2016.

[4] *An Energy Efficient GPGPU Memory Hierarchy with Tiny Incoherent Caches*, Alamelu Sankaranarayanan, Ehsan K.Ardestani, Jose Luis Briz, and Jose Renau, International Symposium on Low Power Electronics and Design (**ISLPED**), September 2013.

[5] *ESESC: a Simulator for Time-Based Sampling of Heterogeneous Multi-threaded Systems*, Ehsan K.Ardestani and Jose Renau, International Symposium on High Performance Computer Architecture (**HPCA**) ,February 2013.

[6] *Thermal-Aware Sampling in Architectural Simulation*, Ehsan K.Ardestani, Elnaz Ebrahimi, Gabriel Southern, and Jose Renau, International Symposium on Low Power Electronics and Design (**ISLPED**), August 2012.

[7] *Enabling Power Density and Thermal-Aware Floorplanning*, Ehsan K. Ardestani, Amirkoushyar Ziabari, Ali Shakouri, and Jose Renau, 28th Annual Thermal Measurement, Modeling and Management Symposium (**SEMITHERM**), March 2012.

[8] *Releasing Efficient Beta Cores to Market Early*, Sangeetha Sudhakrishnan, Rigo Dicochea, and Jose Renau, International Symposium on Computer Architecture (**ISCA**), June 2011.

[9] *Fast Thermal Simulators for Architecture Level Integrated Circuit Design*, Amirkoushyar Ziabari, Ehsan K. Ardestani, Jose Renau, and Ali Shakouri, 27th Annual Thermal Measurement, Modeling and Management Symposium (**SEMITHERM**), March 2011.

[10] *A Design Time Simulator for Computer Architects*, Sangeetha Sudhakrishnan, Francisco J. Mesa-Martinez, and Jose Renau, IEEE International Symposium on Quality Electronic Design (**ISQED**), March 2011. (Best paper award)

[11] *Characterizing Processor Thermal Behavior*, Francisco J. Mesa-Martinez, Ehsan Ardestani, and Jose Renau, Fifteenth International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), March 2010.

[12] *Cooling Solutions for Processor Infrared Thermography*, Ehsan Ardestani, Francisco J. Mesa-Martinez, and Jose Renau, 26th Annual Thermal Measurement, Modeling and Management Symposium (**SEMITHERM**), February 2010.

[13] *Processor Verification with hwBugHunt*, Sangeetha Sudhakrishnan, Liying Su, and Jose Renau, IEEE International Symposium on Quality Electronic Design (**ISQED**), March 2008.

[14] *Effective Optimistic-Checker Tandem Core Design Through Architectural Pruning*, Francisco J. Mesa-Martinez and Jose Renau, 40th International Symposium on Microarchitecture (**MICRO**), December 2007.

[15] *Estimating Design Time for System Circuits*, Cyrus Bazeghi Francisco J. Mesa-Martinez, Brian Greskamp, Josep Torrellas, and Jose Renau, 15th IFIP International Conference on Very Large Scale Integration (**VLSI-SoC**), October 2007.

[16] *Power Model Validation Through Thermal Measurements*, Francisco J. Mesa-Martines, Joseph Nayfach-Battilan, and Jose Renau, 34th International Symposium on Computer Architecture (**ISCA**), June 2007.

[17] *SEED: Scalable, Efficient Enforcement of Dependences*, Francisco J. Mesa-Martinez, Michael C.Huang, and Jose Renau, 15th International Conference on Parallel Architectures and Compilation Techniques (**PACT**), September 2006.

[18] *POSH: A TLS Compiler that Exploits Program Structure*, Wei Liu, James Tuck, Luis Ceze, Wonsun Ahn, Karin Strauss, Jose Renau and Josep Torrellas, ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (**PPoPP**), March 2006.

[19] *uComplexity: Estimating Processor Design Effort*, Cyrus Bazeghi, Francisco J. Mesa-Martinez, and Jose Renau. 38th International Symposium on Microarchitecture (**MICRO**), November 2005.

[20] *POSH: A Profiler-Enhanced TLS Compiler that Leverages Program Structure*, Wei Liu, James Tuck, Luis Ceze, Karin Strauss, Jose Renau, and Josep Torrellas. The Second Watson Conference on Interaction between Architecture, Circuits, and Compilers (**P=AC2**), September 2005.

[21] *Thread-Level Speculation on a CMP Can Be Energy Efficient*, Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti Sarangi, James Tuck, and Josep Torrellas. International Conference on Supercomputing (**ICS**), June 2005.

[22] *Tasking with Out-of-Order Spawn in TLS Chip Multiprocessors: Microarchitecture and Compilation*, Jose Renau, James Tuck, Wei Liu, Luis Ceze, Karin Strauss, and Josep Torrellas. International Conference on Supercomputing (**ICS**), June 2005.

[23] *Programming the FlexRAM Parallel Intelligent Memory System*, Basilio Fraguela, Jose Renau, Paul Feautrier, David Padua, and Josep Torrellas, International Symposium on Principles and Practice of Parallel Programming (**PPoPP**), June 2003.

[24] *Positional Adaptation of Processors: Application to Energy Reduction*, Michael Huang, Jose Renau, and Josep Torrellas, International Symposium on Computer Architecture (**ISCA**), June 2003.

[25] *Cherry: Checkpointed Early Resource Recycling in Out-of-order Microprocessors*, José F. Martínez, Jose Renau, Michael Huang, Milos Prvulovic, and Josep Torrellas, International Symposium on Microarchitecture (**MICRO**), November 2002.

[26] *Energy-Efficient Hybrid Wakeup Logic*, Michael Huang, Jose Renau, and Josep Torrellas, International Symposium on Low Power Electronics and Design (**ISLPED**), August 2002.

[27] *Cache Decomposition for Energy-Efficient Processors*, Michael Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, International Symposium on Low Power Electronics and Design (**ISLPED**), August 2001.

[28] *A Framework for Dynamic Energy Efficiency and Temperature Management*, Wei Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, International Symposium on Microarchitecture (**MICRO**), December 2000.

Journals and Patents

[28] *Managing Mismatches in Voltage Stacking with CoreUnfolding*, Ehsan K. Ardestani, Rafael Trapani Possignolo, Jose Luis Briz, and Jose Renau, ACM's Transactions on Architecture and Code Optimization (**TACO**), September 2015.

[29] *Section Based Program Analysis to Reduce Overhead of Detecting Unsynchronized Thread Communication*, Madan Das, Gabriel Southern and Jose Renau, ACM's Transactions on Architecture and Code Optimization (**TACO**), March 2015.

[30] *Sampling in Thermal Simulation of Processors: Measurement, Characterization, and Evaluation*, Ehsan K.Ardestani, Francisco J. Mesa-Martinez , Gabriel Southern , Elnaz Ebrahimi , Jose Renau IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), August 2013.

[31] *Real-time control for Keck Observatory next-generation adaptive optics*, Marc Reinig, Donald Gavel, Ehsan Ardestani, Jose Renau, Proceedings of the **SPIE**, 2010.

[32] *Using Checkpoint-Assisted Value Prediction to Hide L2 Misses*, Luis Ceze, Karin Strauss, James Tuck, Jose Renau, and Josep Torrellas, ACM's Transactions on Architecture and Code Optimization (**TACO**), March 2006.

[33] *Energy-Efficient Thread-Level Speculation on a CMP*, Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti Sarangi, James Tuck, and Josep Torrellas. IEEE Micro Special Issue: **Micro's Top Picks** from Computer Architecture Conferences, January-February 2006.

[34] *CAVA: Hiding L2 Misses with Checkpoint-Assisted Value Prediction*, Luis Ceze, Karin Strauss, James Tuck, Jose Renau, and Josep Torrellas, IEEE TCCA Computer Architecture Letters (**TCCA**), December 2004.

[35] *Managing Multiple Low-Power Adaptation Techniques: The Positional Approach*, Michael Huang, Jose Renau, Josep Torrellas, Sidebar, IEEE **Computer Magazine**, December 2003.

[36] *A Framework for Dynamic Energy Efficiency and Temperature Management*, Wei Huang, Jose Renau, and Josep Torrellas, Journal on Instruction Level Parallelism (**JILP**), October 2001.

[37] Oracle Patent, Combining a Remote TLB Lookup and a subsequent Cache Miss into a Single Coherence Operation. ORA12-0263-US-NP

[38] UCSC Patent application, Long Latency Tolerant Decoupled Memory Hierarchy for Simpler and Energy Efficient PCT/US2012/070046

Workshops and Posters

[39] *Section Based Program Analysis to Reduce Overhead of Detecting Unsynchronized Thread Communication*, Madan Das, Gabriel Southern, and Jose Renau, 20th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP Poster), February 2015

[40] *Deterministic Scaling*, Gabriel Southern, Madan Das, and Jose Renau, Workshop on Determinism and Correctness in Parallel Programming (WODET), March 2013.

[41] *Reducing Logging Overhead for Deterministic Execution*, Gabriel Southern, Madan Das, and Jose Renau, Workshop on Determinism and Correctness in Parallel Programming (WODET), March 2013.

[42] *ReRack: Power Simulation for Data Centers with Renewable Energy Generation*, Michael Brown, and Jose Renau, GreenMetrics 2011,held in conjunction SIGMETRICS 2011, June 2011.

[43] *SOI, Interconnect, Package, and Mainboard Thermal Characterization*, Joseph Nayfach-Battilana and Jose Renau, Poster with proceedings at International Symposium on Low Power Electronics and Design (ISLPED), August 2009.

[44] *Measuring and Modeling Variability using Low-Cost FPGAs*, Michael Brown, Cyrus Bazeghi, Matthew Guthaus and Jose Renau, Poster with Proceedings at the International Symposium on Field-Programmable Gate Arrays (FPGA), February 2009.

[45] *Measuring and Modeling Variability using Low-Cost FPGAs*, Michael Brown, Cyrus Bazeghi, Matthew R. Gutthaus, and Jose Renau, Workshop on Modeling, Benchmarking and Simulation (MOBS), held inconjunction with ISCA-36, June 2009.

[46] *Implementation of a Power Efficient High Performance FPU for SCOORE*, Wael Ali Ashmawi, John Burr, Abhishek Sharma, Jose Renau, Workshop on Architectural Research Prototyping (WARP) held in conjunction with ISCA, June 2008.

[47] *Measuring Power and Temperature from Real Processors*, Francisco-Javier Mesa-Martinez, Michael Brown, Joseph Nayfach-Battilana, Jose Renau, The Next Generation Software (NGS) Workshop (NGS08) held in conjunction with IPDPS, April 2008.

[48] *uDSim, a Microprocessor Design Time Simulation Infrastructure*, Sangeetha Sudhakrishnan, Francisco-Javier Mesa-Martinez, Jose Renau, Wild and Crazy Ideas VI (WACI) held in conjunction with ASPLOS, March 2008.

[49] *Printed Circuit Board Layout Time Estimation*, Cyrus Bazeghi and Jose Renau, 7th Workshop on Complexity-Effective Design (WCED), held in conjunction with ISCA-33, June 2006.

[50] *SCOORE: Santa Cruz Out-of-Order RISC Engine, FPGA Design Issues*, Francisco J. Mesa-Martinez, Abhishek Sharma, Andrew W. Hill, Carlos A. Cabrera, Cyrus Bazeghi, Hari Kolakaleti, Joseph Nayfach, Keertika Singh, Kevin S. Halle, Matthew D. Fischler, Melisa Nunez, Sangeetha Nair, Suraj Narender Kurapati, Wael Ali Ashmawi, and Jose Renau , Workshop on Architectural Research Prototyping (WARP), held in conjunction with ISCA-33, June 2006.

[51] *Profile-Based Energy Reduction for High Performance*, Wei Huang, Jose Renau, and Josep Torrellas, ACM Workshop on Feedback-Directed and Dynamic Optimization (FDDO), December 2001.

[52] *Energy/Performance Design of Memory Hierarchies for Processor-In-Memory Chips*, Wei Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, Workshop on Intelligent Memory Systems, November 2000. It also appeared in Lecture Notes in Computer Science (Vol. 2107) by Springer-Verlag, 2001.

[53] *Memory Hierarchies in Intelligent Memories: Energy/Performance Design*, Wei Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, Ninth Workshop on Scalable Shared Memory Multiprocessors, June 2000.

Profesional Activities and Memberships

- Vice General Chair: HotChips 2016
- Program Chair: ISPASS 2015
- Program Chair: HotChips 10 co-chair
- Local Chair: PPoPP/CGO/HPCA 2015, VLSI-SoC 2013
- Program Committee service: HPCA 16, ISPASS 16, ISPASS 14, ISPASS 12, SC 13, ISCA 11, HotPower 10, MICRO 09, ICPP 09, HotChips 09, ICCD 09, ICCD 08, HotChips 08, ICCD 07, IPDPS 07, ICCD 06
- Host MURN Kickoff 2011 retreat at UC Santa Cruz.
- Host the RAMP 2010 January retreat at UC Santa Cruz.
- Guest editor for IEEE MICRO March/April 2011 edition.
- NSF Panels: 2015, 2014, 2013, 2012, 2006